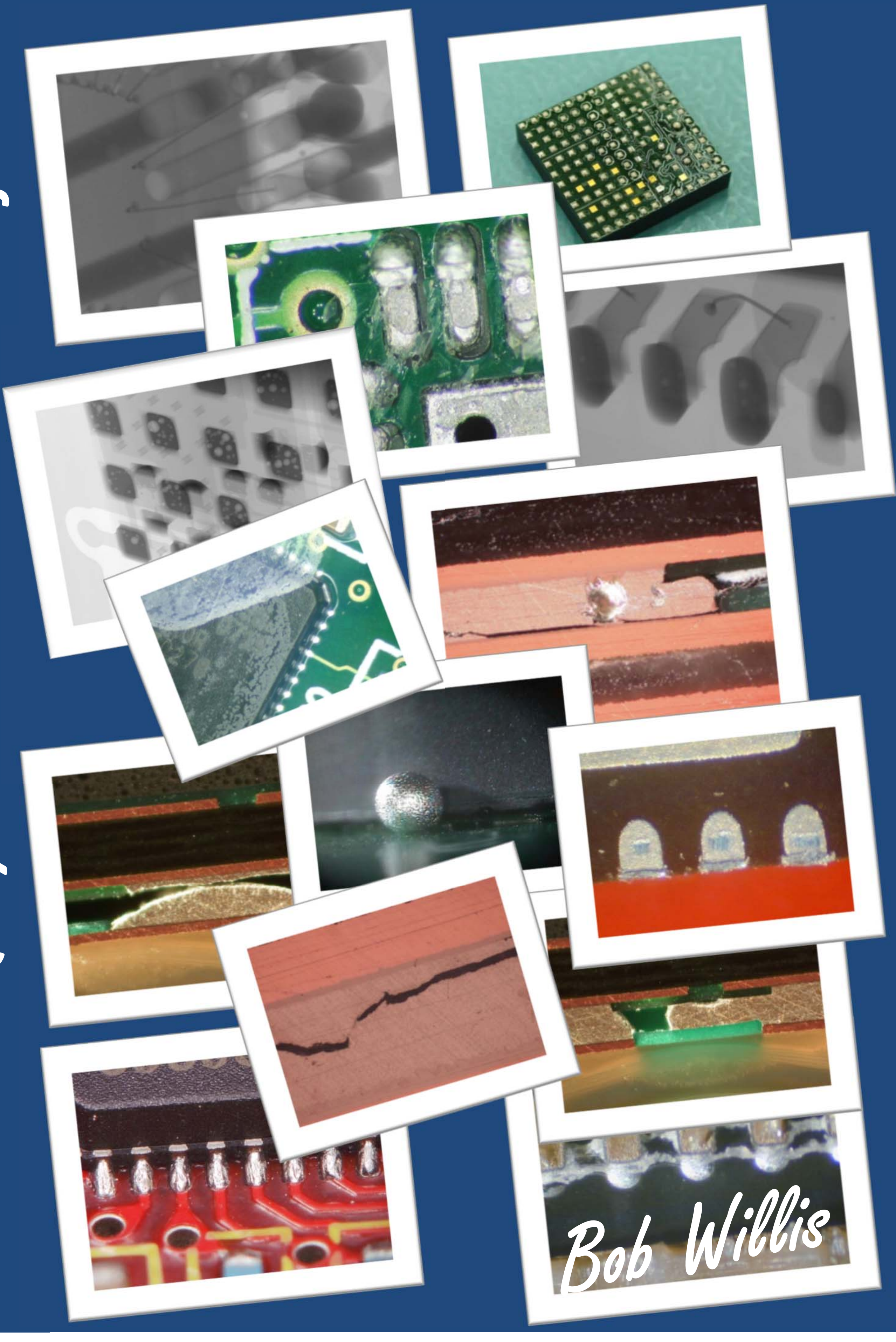
Guide to QFN/LGA & BTC Process Defects



Bob Willis

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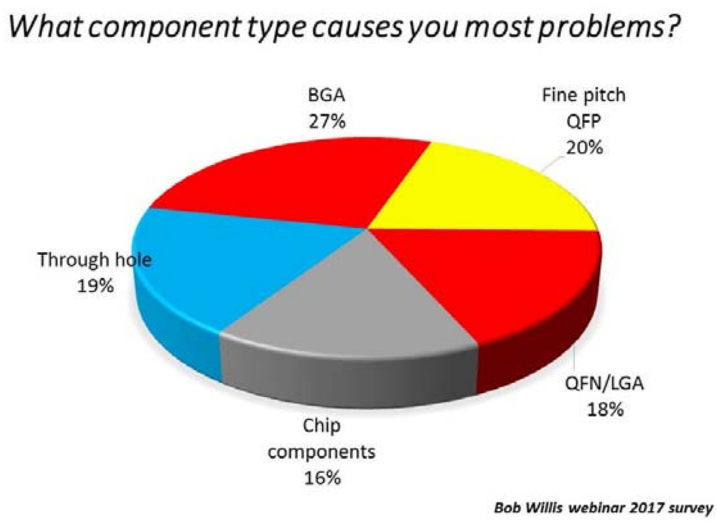
Introduction

Welcome to this Process Defect Guide on QFN/LGA & Bottom Mounted Components

Our latest Process Defect Guide, is aimed at QFN/LGA components, what IPC refer to as Bottom Mounted or Bottom Termination Components. The parts were introduced to industry a few years ago and their use has increased significantly in many industry sectors. The cost to produce these packages is more cost effective than their leader alternatives, they take up less space and are more robust. Like any new package they do introduce new challenges to assembly staff. Its important to run trials and make design, assembly and quality staff aware of any special requirements before running in high volume. Always have a procedure in place for good New Product Introduction (NPI)

Our latest webinar survey of 100 engineers shows that QFN/LGA parts are a common cause of process problems for users; however BGA, QFP and through hole still create more issues. The main point of discussion with these parts is voiding, which may not be an issue to users. More recent use in more demanding environments has also illustrated that long term thermal cycling performance may still be an issue due to cracking of edge joints



With information to help newcomers and expert users we hope you find the guide useful and ask you to pass on this knowledge to your team, your customers and suppliers. If you have any other defect types why not add them to the **NPL Defect Database** http://defectsdatabase.npl.co.uk or send them to technical@smartgroup.org

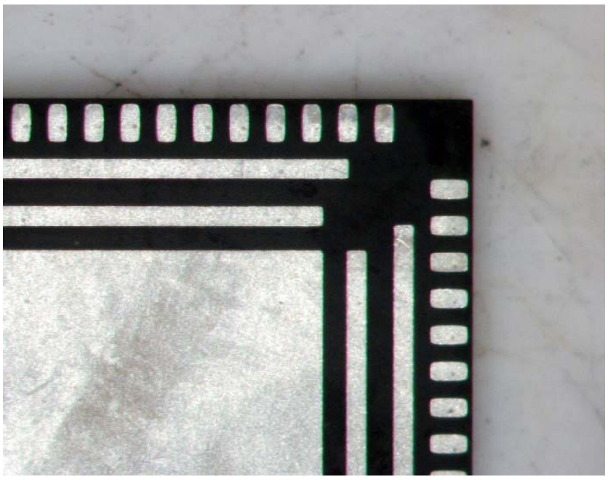
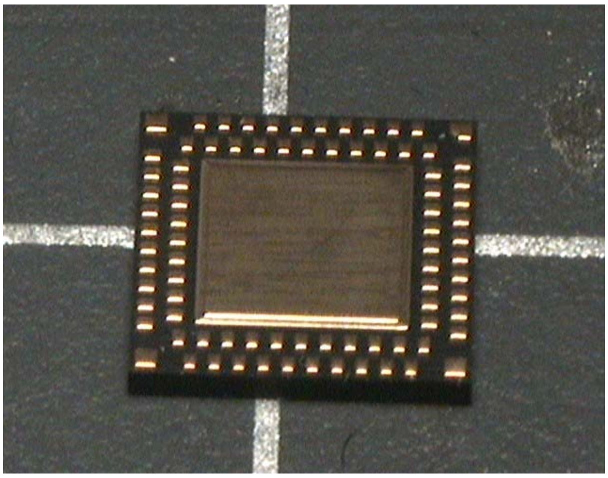
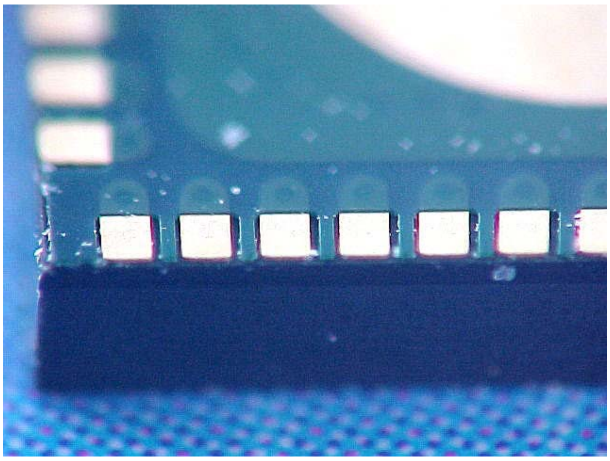
Many thanks again for your support

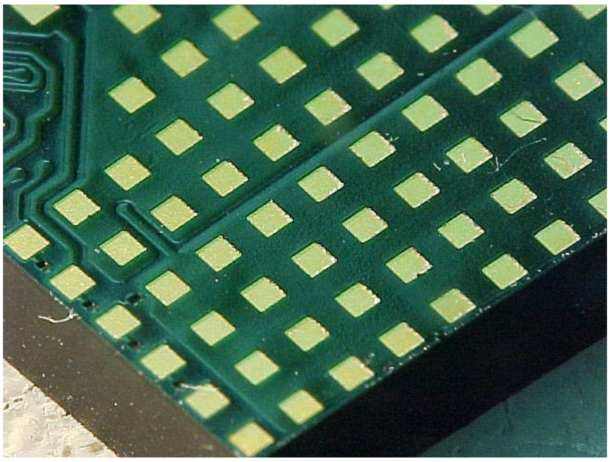
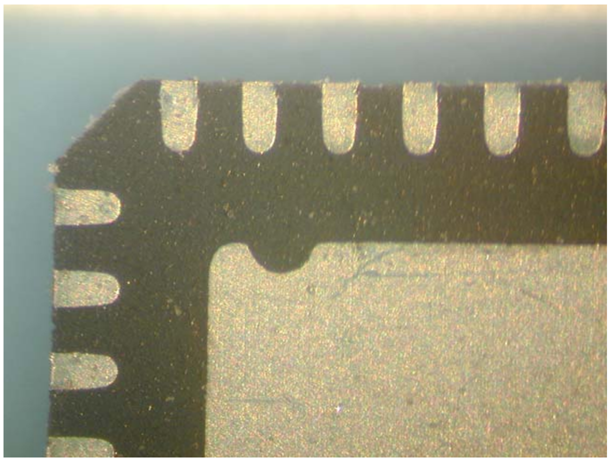
Bob Willis
SMART Group Technical Committee Member

QFN LGA Component Package Examples

Quad Flat No Lead (QFN) & Land Grid Array (LGA) are the most common terms used in industry to describe these types of components and have been around since they were first introduced around 2000. Other names and abbreviations have been used but often by marketing departments to differentiate their company parts from the rest. The IPC standard, IPC 7093 Design & Assembly Process Implementation for Bottom Termination Components first introduced in 2011 tried to use one common term to avoid confusion Bottom Termination Component (BTC)

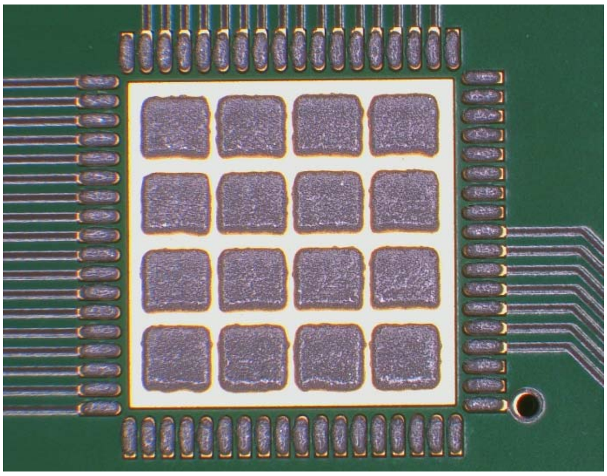
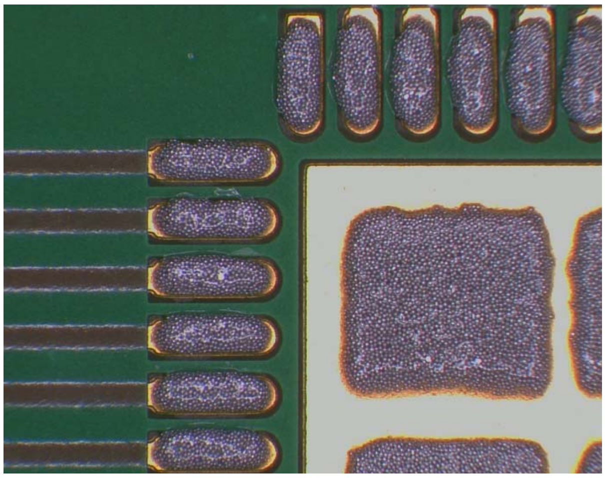
The following images illustrate a small range of the parts that are currently used in the industry, there will be more in the future

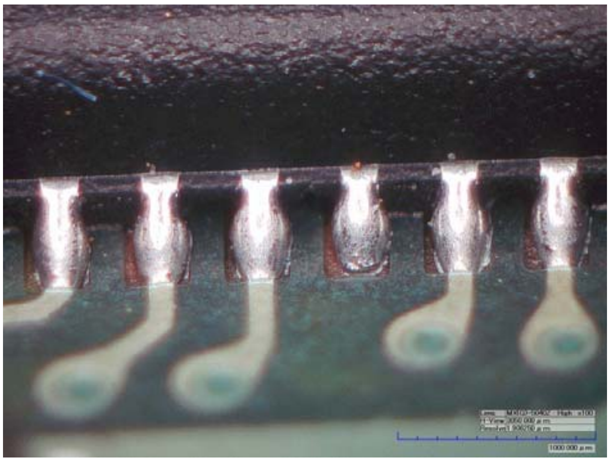
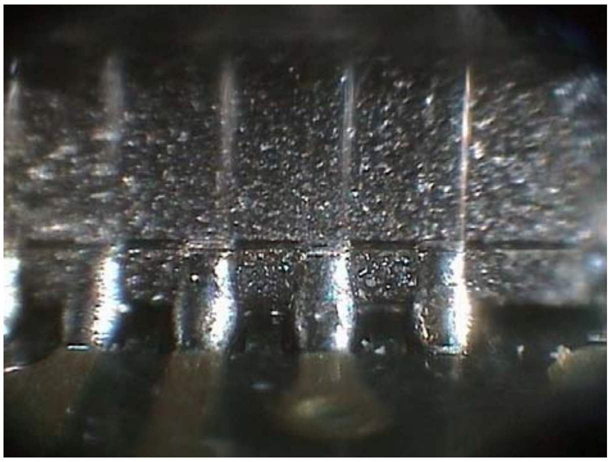
QFN/LGA Reference Solder Joint Images

Satisfactory Solder Paste Deposit

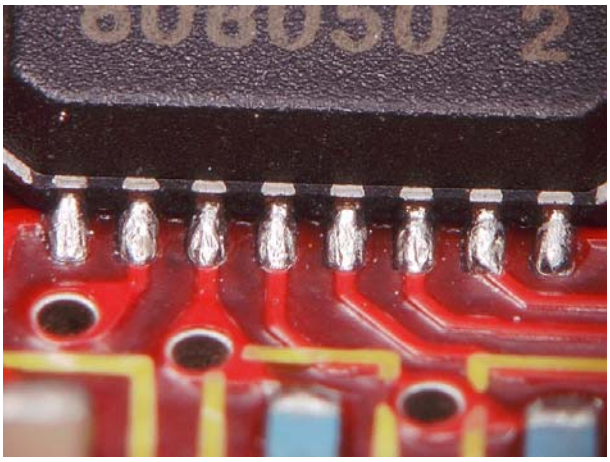
Solder paste has been printed successfully on the outer pads and centre pad. The stencil thickness used in the example would appear to be thicker than required for a package of this size and pitch. However, the results from the production line were satisfactory, using both convection and vapour phase reflow. Reducing the total paste volume on the centre pad by decreasing the number of segments in the stencil did reduce voids

Satisfactory Solder Joints

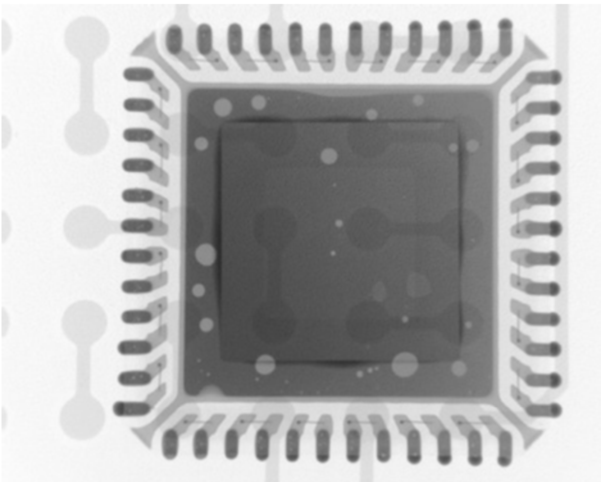
Both the images above show satisfactory solder joints formed during reflow with good wetting to the side terminations. There is no requirement for solder fillets to the side of the parts under IPC standards due to the lack of wetting on these parts during their early introduction. Some vendors have been successful in improving their process, changing the singulation method or changing the lead frame and plating steps

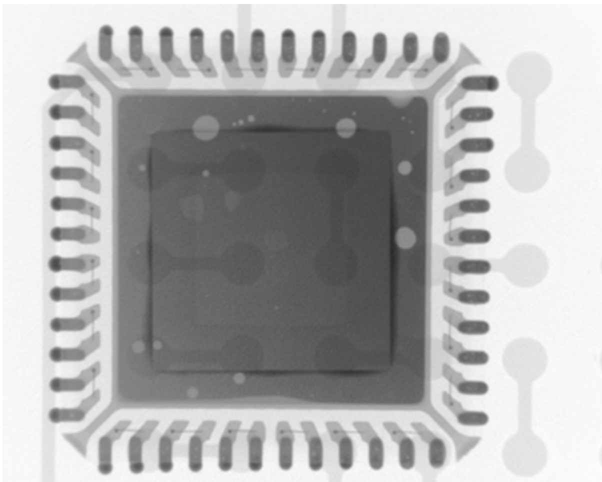
Satisfactory Solder Joints



The solder joints above are again satisfactory with reduced wetting on the side lead frame which is typical of parts that do have some level of side solderability. Having designs that allow formation of side solder fillets allows for Automatic Optical Inspection (AOI) and easier rework and repair, touch up of single joints and is good practice. The formation of side fillets may also slightly improve the reliability during temperature cycling

Satisfactory Solder Joints

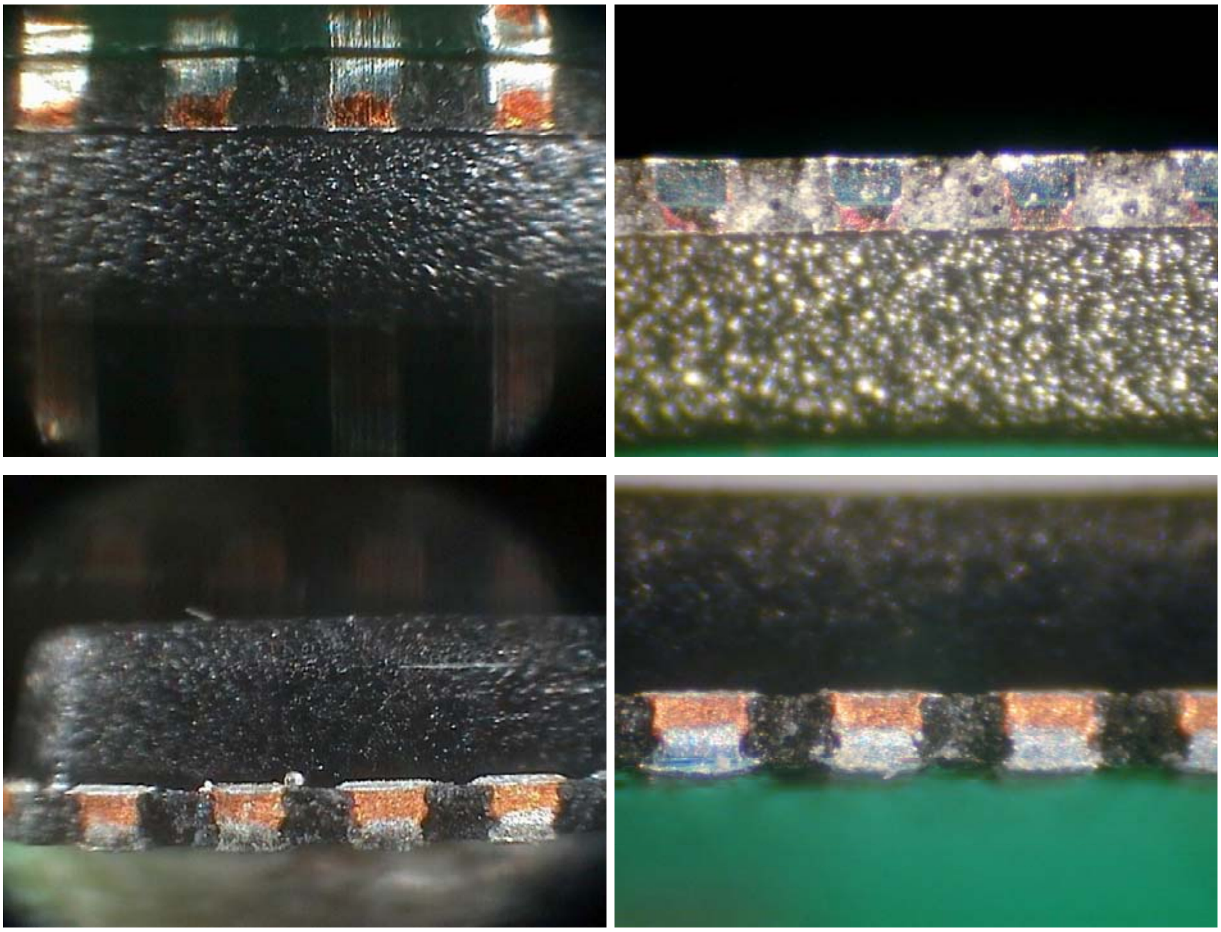




The x-ray images show examples of what would be considered satisfactory soldering of QFN packages with minimum voids under the centre pad or in the outer pads. The images were created by Dr David Bernard and the author in the first guide to x-ray inspection and published by DAGE in 2006 during the introduction of lead-free. Two sets of inspection and quality control posters featuring optical and x-ray for area array termination are available from the SMTA www.smta.org

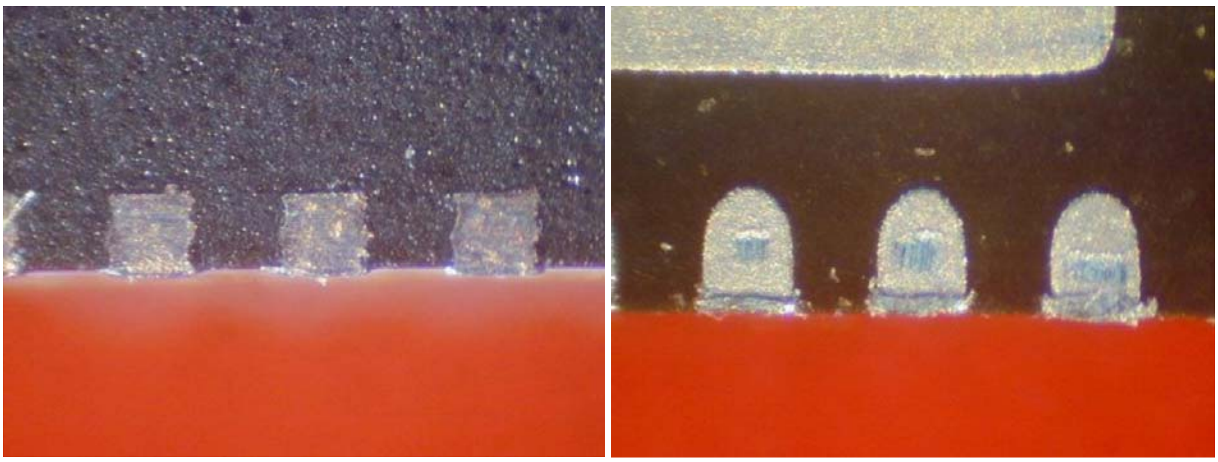
QFN/LGA Process Defects & Potential Causes

Smeared Tin Plating



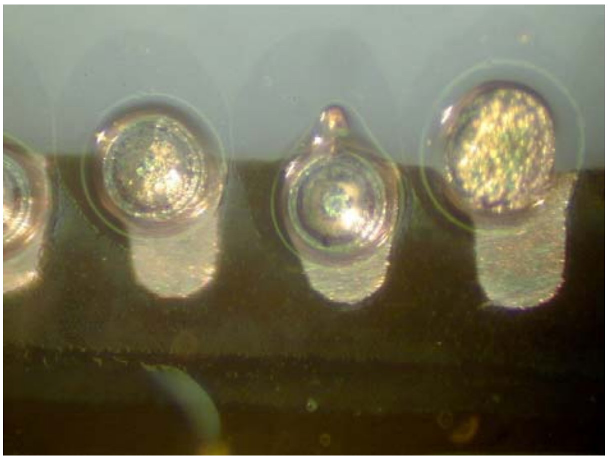
Smearing of the tin plating on the cut surface of the QFN/LGA lead frames does allow wetting during reflow but is variable. Unfortunately, it often leads to poor wetting and in some case solder slivers on the plastic body of the device which is poor manufacturing quality control. These slivers may be lost during assembly and reflow but if seen at goods receipt it demonstrates poor process control during component manufacture and should be highlighted to the component supplier

Tin Plating Slivers & Burrs



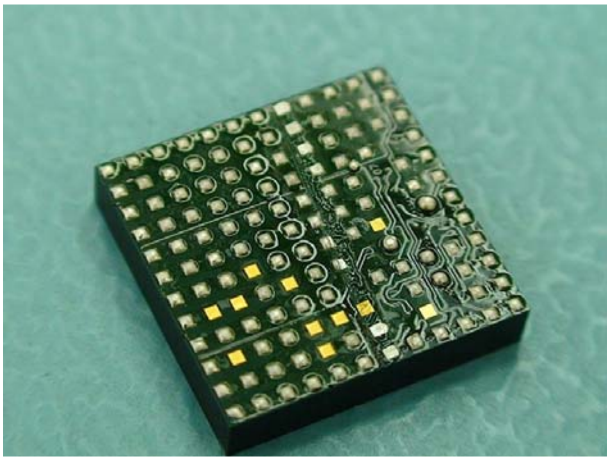
The image opposite on the left shows tin plating slivers on the body of the component, during early introduction we have experienced these slivers between the terminations by as much as 50%. The right image shows burrs on the terminations which are not uncommon but are again an indication of poor manufacturing control. These are often noted during sectioning of joints but have never been shown to be an issue. The method of component singulation, direction or the tooling maintenance need to be reviewed

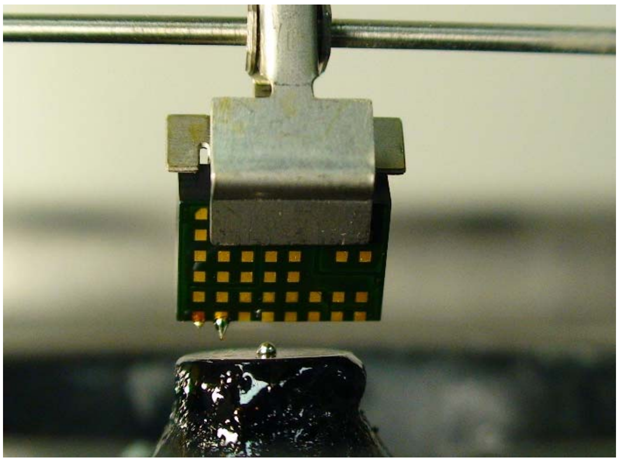
Poor Termination Solderability



The package shows poor solder wetting on the terminations. Although you can test parts with a wetting balance and this has been successfully demonstrated by the author, it is often quicker to do a process simulation test with solder paste. Paste is printed on to a glass microscope slide, the component placed and reflowed. All the paste should reflow on each termination showing perfect wetting, not as the example has shown when inspected through the glass. A procedure for test with photographs is available as a set of QFN/LGA posters on line from the SMTA www.smta.org

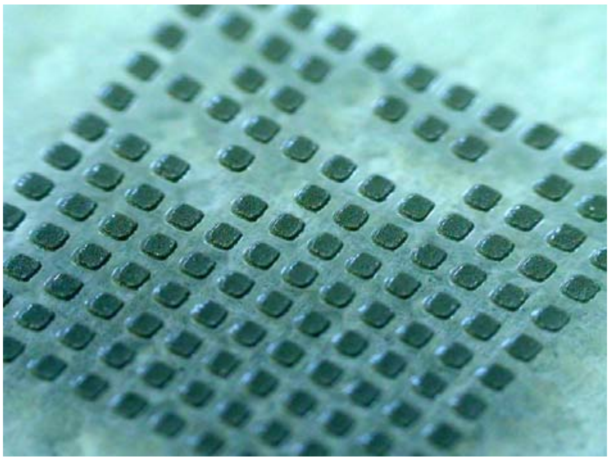
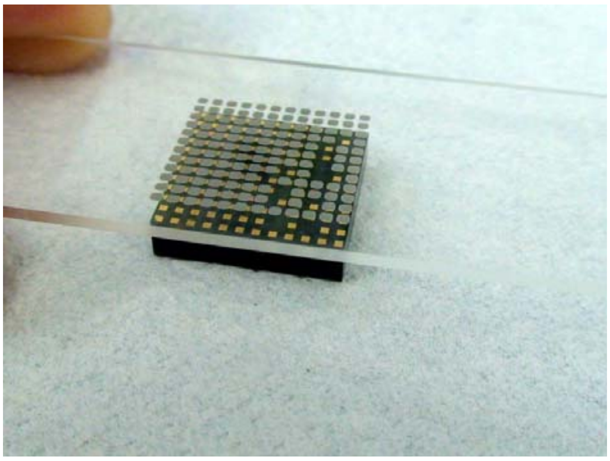
Poor Solderability Testing Method



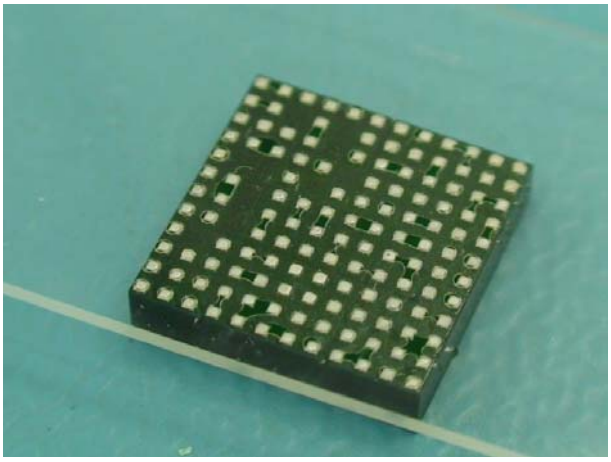
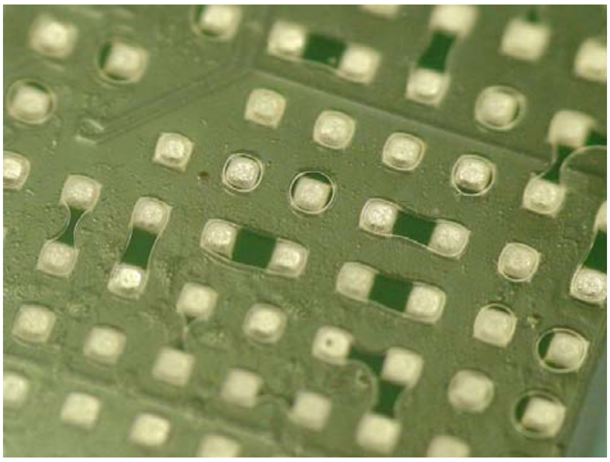


Solder dip or float testing is often used in the industry as it is quick and simple; however it can lead to incorrect assessment as found on this part. The solderability of the terminations was good but the test method for this design is not appropriate. The correct and simple way is to use paste and a glass plate as a process simulation test covered in IPC standards. Alternatively, the wetting balance can be used on the edge pads as this gives the best opportunity to directly measure the wetting force and easier to align the sample and solder pellet. Longer pre-heat is required on parts of this type due to its high mass. Testing component shown above on the right

Process Simulation Solderability Testing

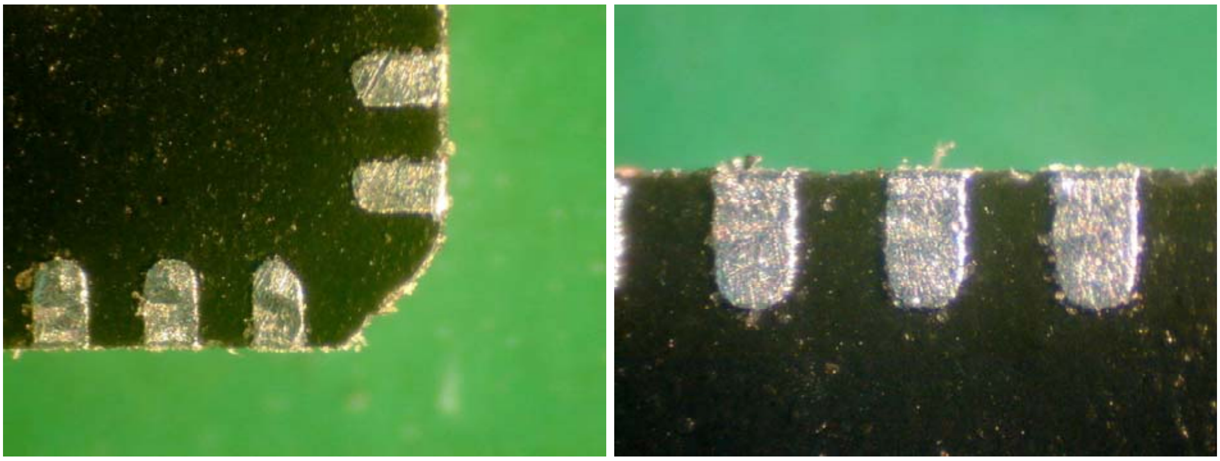
 

Paste is printed using the original stencil used in production on to a glass slide. The slide is then turned upside down and place on to the component aligning the paste to the terminations before turning over. Care needs to me taken based on the weight of the component. Simple 40 pin QFN/LGA parts are OK the tack of the solder paste will hold them in place. The example shown is heavier and care needs to be taken when picking up and turning the glass slide

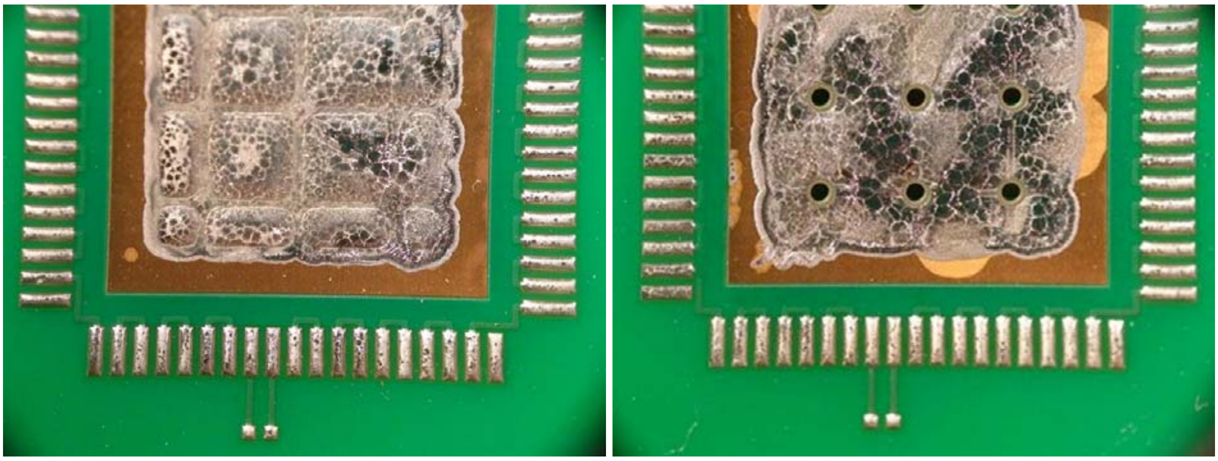
The images above show satisfactory wetting to the terminations after reflow. The close-up image on the right shows the terminations and the flux from the paste between the component and glass slide. All terminations have wetted well with solder and should provide satisfactory yield during assembly. This test method is far better and more representative of reflow technology when compared to dipping a part in to a bath of solder

Uneven Termination Plating



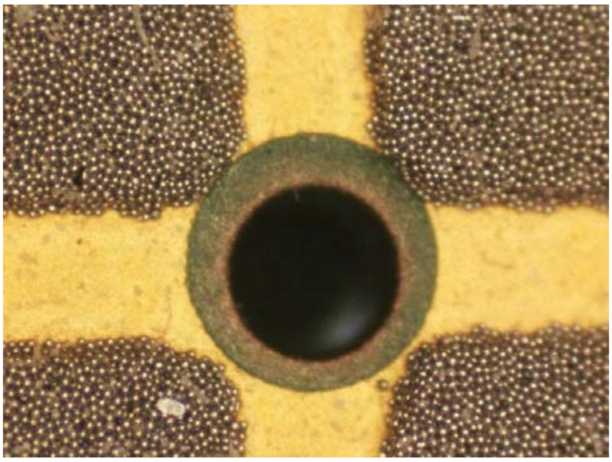
The quality and consistency of the plating on the terminations is poor which did lead to poor results during solderability testing. Reflowing the parts also showed some evidence of outgassing from the plating which can occur when the plating bath is poorly maintained. Plating outgassing can lead to voids in the solder joint, micro voids at the termination interface

Solder Paste Reflow with Vias



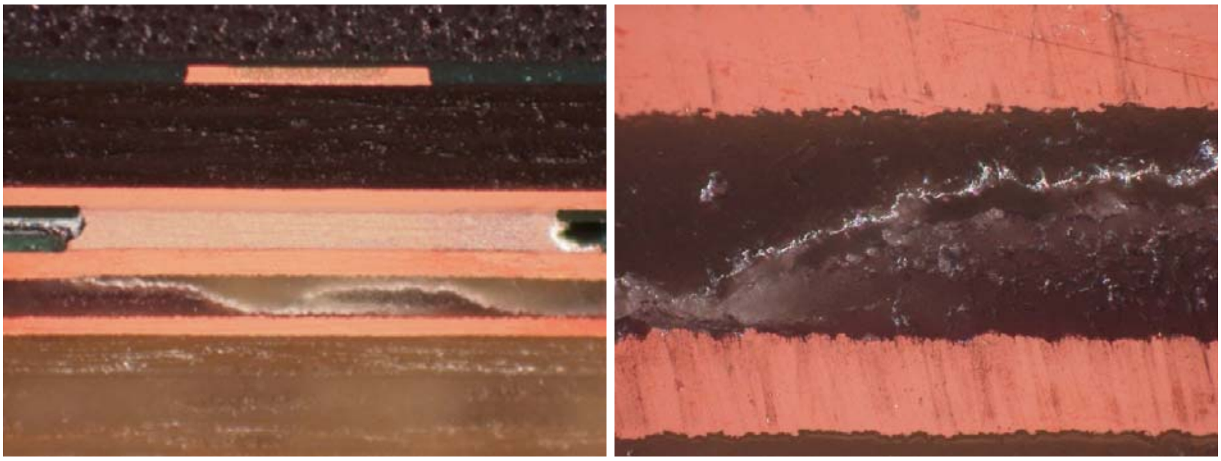
Two QFN examples above show comparisons between soldering with and without through vias in the centre pads. The difference is the correct paste stencil design and the use of solder mask around the vias. This prevents the solder being lost to the vias and has been shown to reduce void formation during reflow with convection and vapour phase soldering but without the need for vacuum

Design with Blind or Through Vias



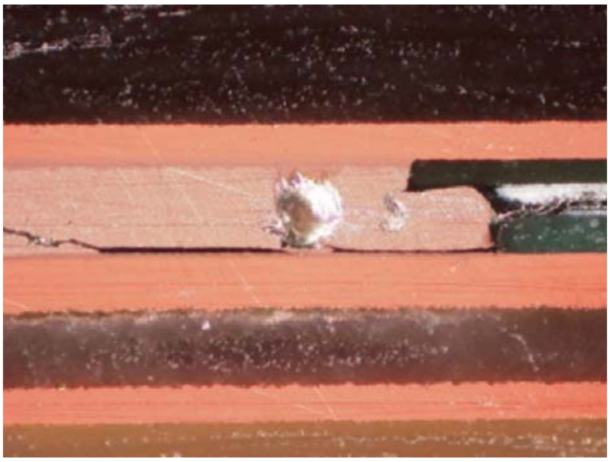
Close up of a through via with solder mask filling the via and the solder paste printed with a segmented pattern and covering approximately 40-50% of the centre pad. It is normally possible to reduce the volume further to reduce the amount of volatile material from the paste during reflow. Ideally its better to have solder mask imaged and developed with rings around the vias rather than filling the vias. This increases the ability for any volatile to escape during soldering but still prevents the solder filling the vias

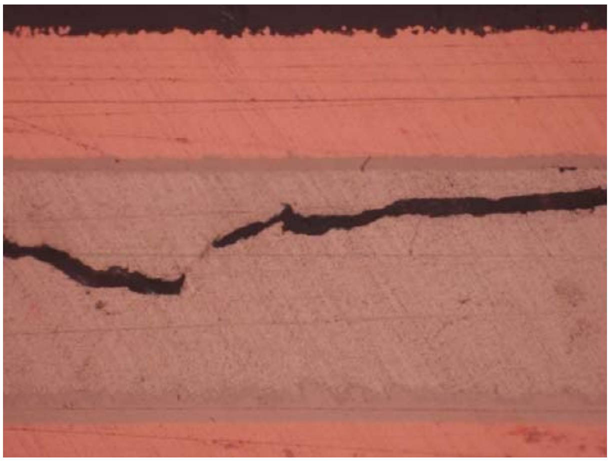
PCB Laminate Cracking



Cracking or separation of the laminate has been seen on some base materials during and after the introduction of lead-free. Experience shows that some materials are brittle leading to the epoxy cracking, which is one of the reasons we have seen pad lifting on BGA packages. We have also seen more evidence of this failure during flexure of boards or during drop testing, again more likely with some specific laminates. Any cracking of separation of the glass and the epoxy in the laminate can lead to CAF failures. Basically CAF Conductive Anodic Filament is where there is a lowering of the insulation along the path of the crack or separation. Detailed reports on the formation of CAF and some methods of preventing this failure mode are available from the NPL Defect Database Online

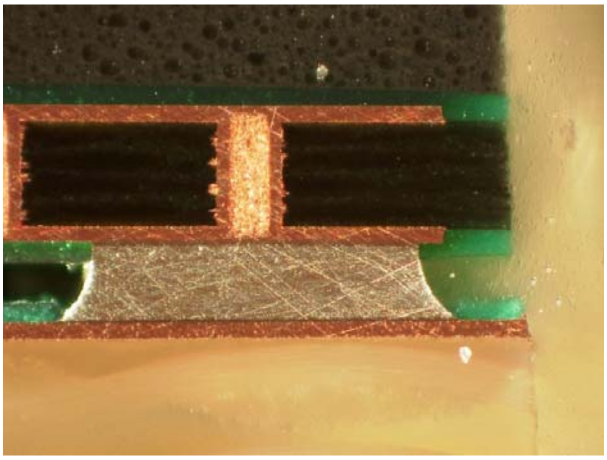
Solder Joint Failure & Laminate Cracking





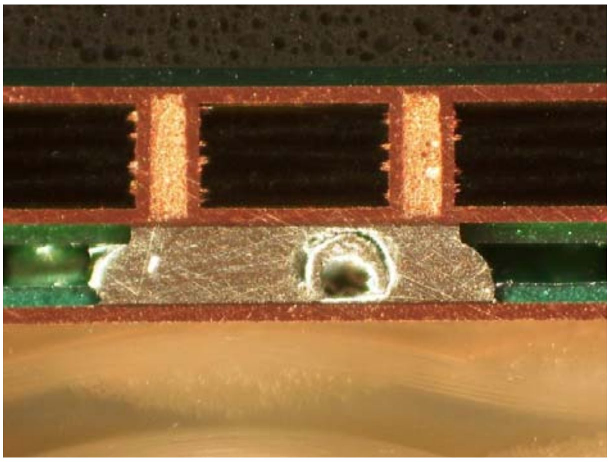
In the examples above, we show evidence of solder joint separation from the pad and lifting of the pad away from the epoxy resin. We also see cracking in the bulk of the solder between the component and the PCB. This type of failure is more likely to be found after mechanical testing with drop testing or flexture

Satisfactory Solder Joint



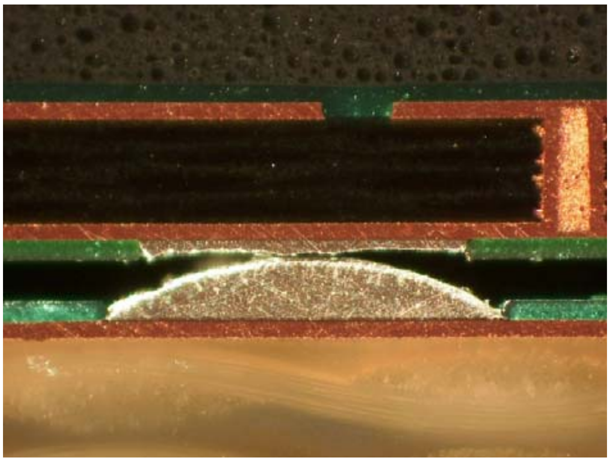
The microsection shows a satisfactory joint on a BTC component provided by Linear. The solder paste is printed on the board and the component with square termination with a gold finish are placed on the surface of the paste prior to reflow. Due to the way the components are made with thick solder mask defined pads many engineers struggle to reflow without a lot of voiding or in some cases open joints. In this case some users have bumped the packages first as part of a pre-assembly process before reflowing with flux gel

Voids in Solder Joint



Microsection shows a BTC device from Linear with a void in the bulk of the solder joint. The void size is within IPC guidelines but could be reduced with more process engineering trials

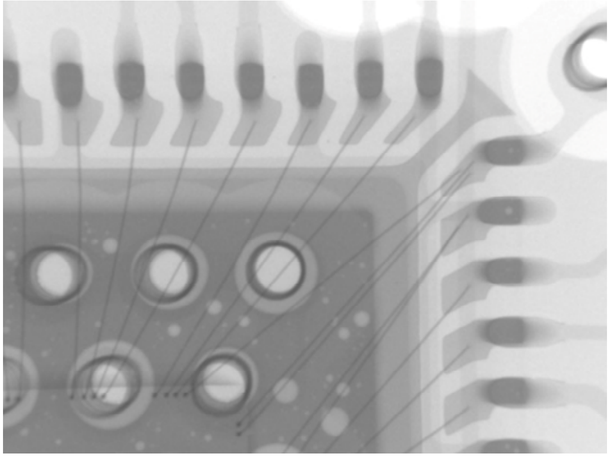
Open Solder Joint



Open solder joint on this BTC area array package was simply caused by poor paste volume control. The volume of solder was not sufficient to create a joint. As there was evidence of solder wetting the component pad the device was in contact with the paste during initial reflow. It is assumed that the wetting to the PCB pad was faster than the component termination and that is the reason for the separation. It may be the case that variability in the solder volume on multiple pads may have caused the package to tilt and float leading to separation. Equally if there was a high level of volatility during reflow this may have contributed to the open joint

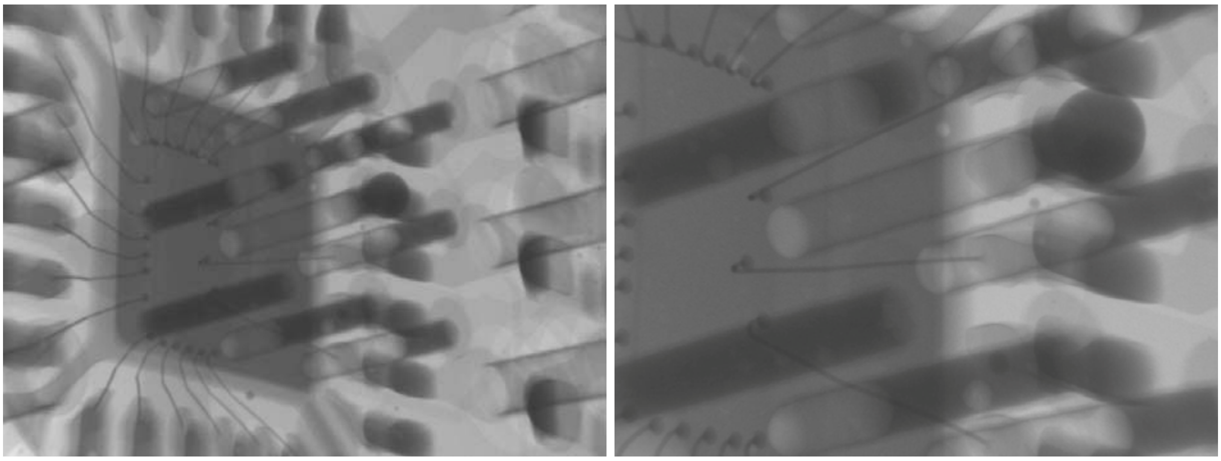
Details and some video examples on Failures are featured on YouTube using the following Video Link

Satisfactory QFN Joints



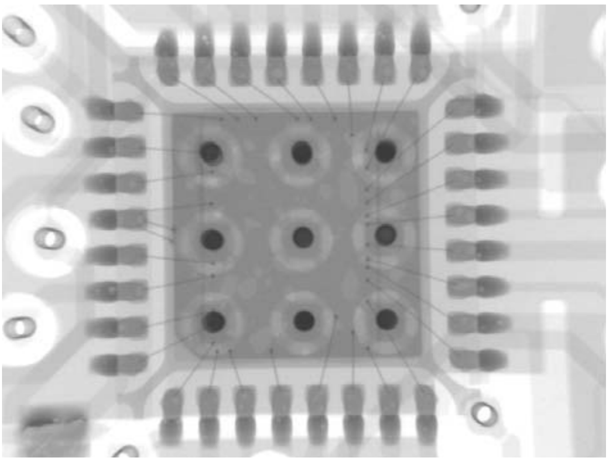
The x-ray images show satisfactory joints on the outer contacts and very limited voiding on the centre pad after reflowing. The white rings around the via holes are the solder mask donuts to prevent solder paste wetting into the vias and away from the centre pad. Although the wetting is good on the edge pads on the base of the device there are limited side fillets. This may be the volume of paste printed, the stencil design or lack of edge wetting on the device. Even if the packages are known to have either poor or no wettable flanks the pad design and stencil aperture size should allow for paste and wetting beyond the edge of the packages

Solder Balls/Balloons



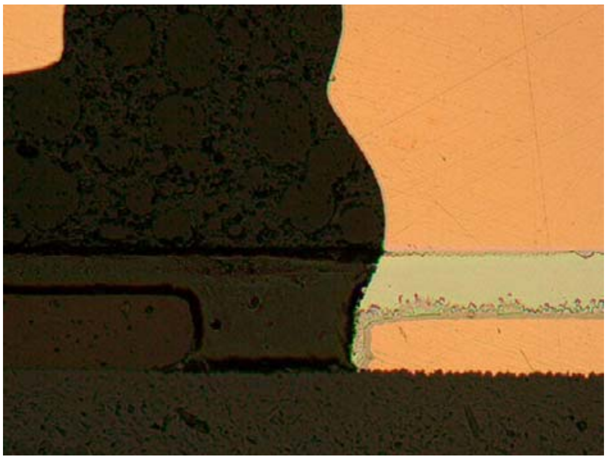
Poor design and assembly process has allowed the solder paste to reflow unevenly on the centre pad and, in some cases reflow through the via holes which is very poor practice. Taking solder volume away from the package reduces stand off height and may cause the device to tilt and possibly create shorts. If the package is assembled on side one of a double sided design it would also make solder paste printing on side two impossible due to the solder balloons on the vias

Satisfactory QFN Joints



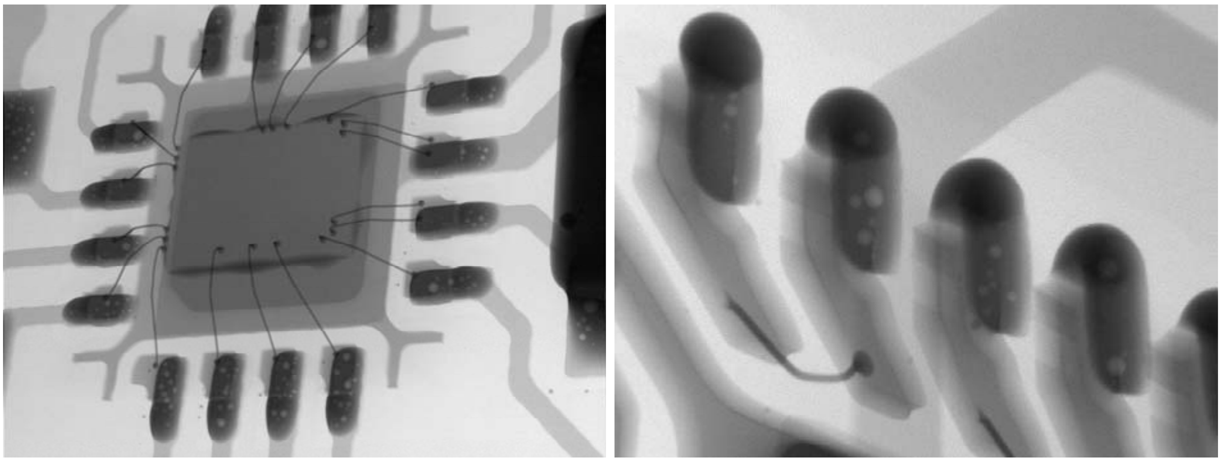
The x-ray image shows good wetting and minimum voiding after reflow. The volume of solder on the active pin on the edge of the package does vary and does extend away from the package sides. The design has incorporated thermal breaks on the vias under the centre pad

Satisfactory QFN Joints



A microsection has been taken to look at the joint formed under a QFN package. The section shows a perfectly good solder joint between the component termination and a surface pad. The intermetallic formation between the PCB pad and the bulk solder is satisfactory, the intermetallic is a tin/nickel as the board being used was gold over nickel

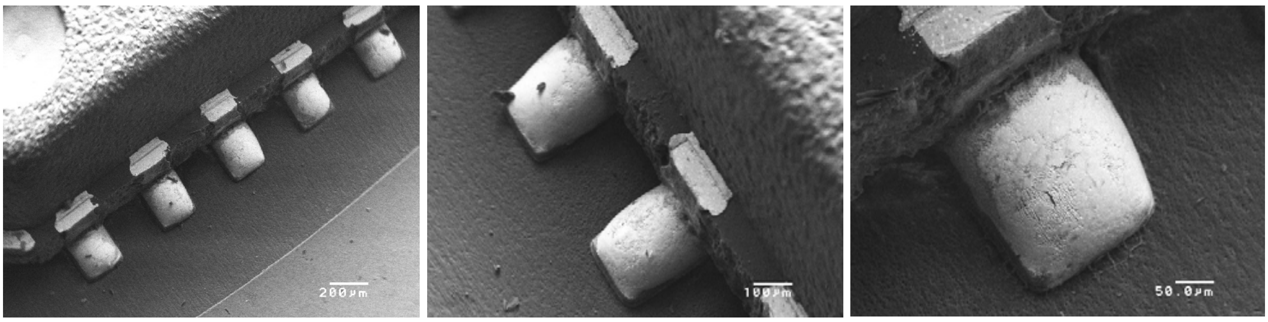
Satisfactory QFN Joints



X-ray images show satisfactory solder joints on the QFN package. The closeup joints to edge of the package show good wetting to the base of the lead frame and to the edge of the package where wettable surfaces must be present. There is some voiding in the peripheral terminations but less than recommended based on IPC standards

Looking under the QFN it is possible to see some small solder balls visible around the joints but not of a size to reduce the insulation resistance or cause an issue. The small balls may have been caused by the printing process or by excess placement force of the components

Failure of QFN Joints

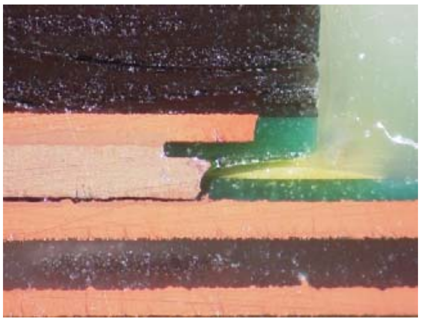
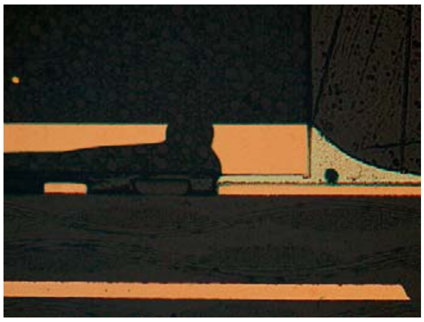


Solder joint failure may occur for several reasons. They are experienced due to:

Differential thermal expansion of board and component
Flexure or dropping testing substrates
Coating/encapsulate expansion

The rate that solder joints have been found to fail is due to thermal expansion of the solder alloy, joint height, temperature range, size of package, size of die in package. These reasons for failure also relate to the design of the product and the thickness of the substrate. To confirm product reliability for a specific environment, engineers do need to undertake some reliability assessments on any new component types and alloy combinations. The SEM images above were taken after 1000 cycles between 125°C to -55°C with no apparent visual damage. Microsections did detect some level of cracking in selected joints

Failure of QFN Joints

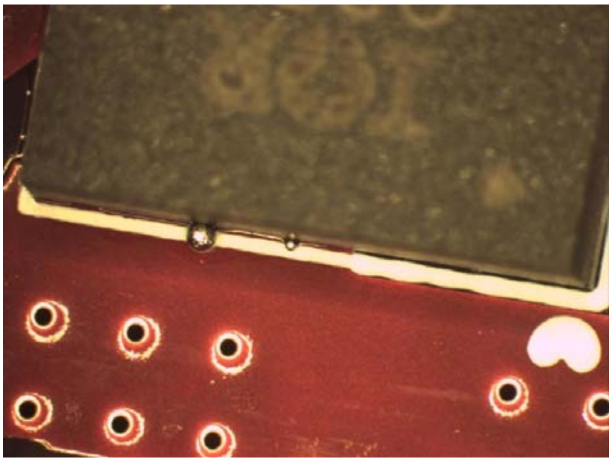
The examples above show full or partial joint failure during investigation or introduction of parts on different products

Example on the left above was on a part subjected to drop testing and the failure has occurred just above the solder joint intermetallic with SAC alloy on a nickel gold board

Centre image shows cracking on a flexible circuit using SAC alloy. In this case the flexible circuit was incorrectly allowed to continually flex during temperature cycling, not intended in the product application

Example on the right is initial separation during standard temperature cycling where a previously satisfactory joint starts to show cracking between the base of the outer termination and the joint on the outer edge

Solder Beads

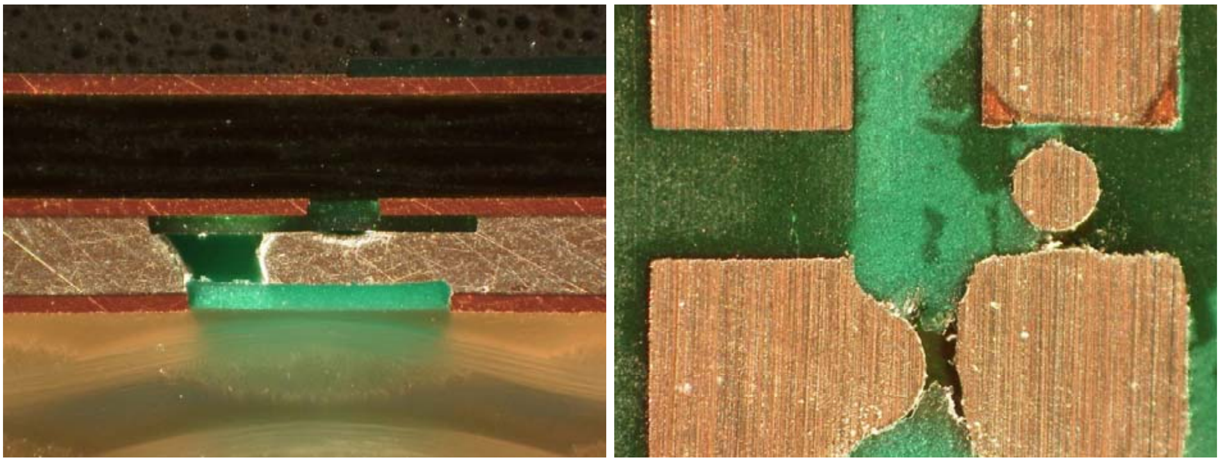
 

The two examples of solder beads after reflowing are related to placement force prior to reflow where the solder paste deposit is displaced away from the pads before reflow soldering. It is uncommon but the solder beads have also been seen to come out from the package itself due to excessive heat during reflow

Solder Squeeze Out

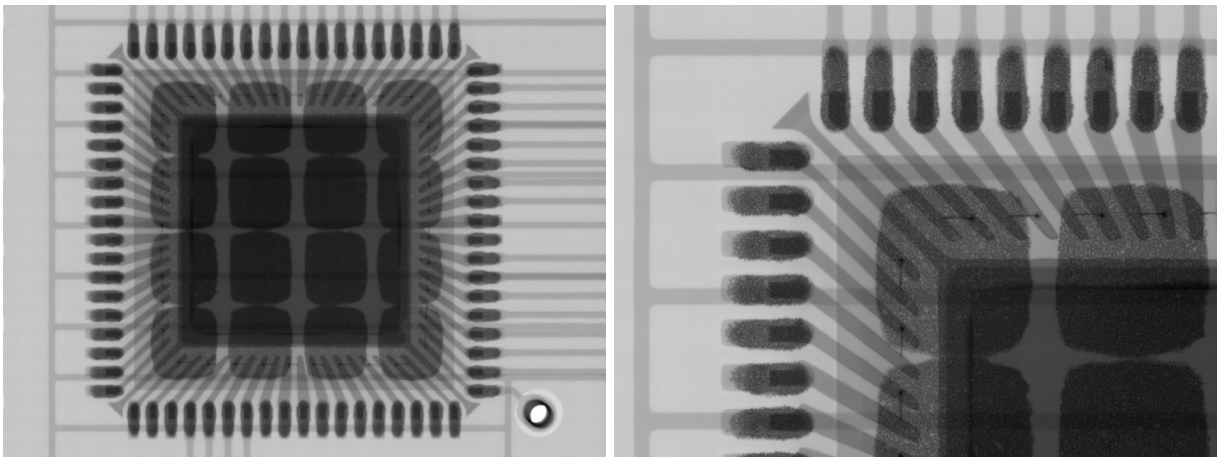
Solder beads or balls on the side of packages and close to the board surface are related to paste printing, paste volume, stencil design, PCB pad size, placement force or reflow and can easily be demonstrated. The example here is different as the solder has squeezed out of the component body during reflow. Lead-free solder has reflowed internally and been forced out of the package. It is most likely to have also migrated to other areas of the component and the circuit creating other potential failure modes

Solder Squeeze Out

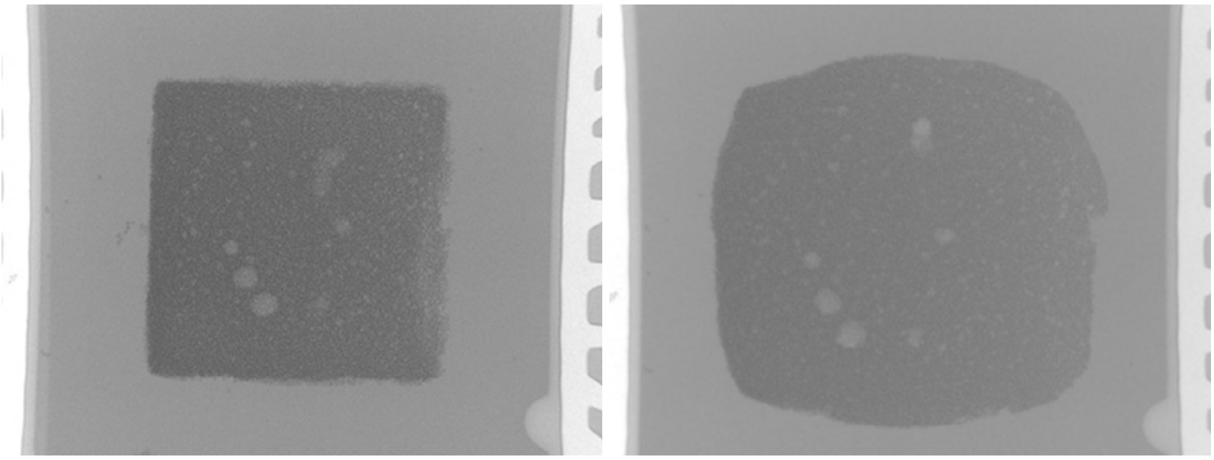


Microsections taken under a package show squeeze out of solder paste which then reflows between terminations. Sometime the solder deposit is isolated between pads, or a solder sausage, as some UK engineers have called it. This may be caused by paste volume variations, excess placement pressure or sometimes warping of the component

Solder Paste Displacement

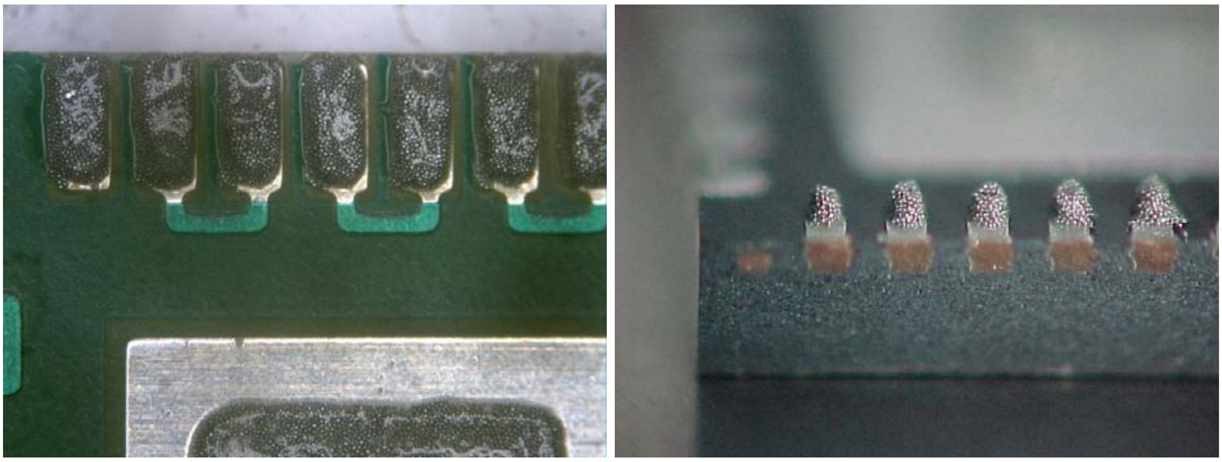


When setting up a process for Package on Package (PoP) or QFN/LGA devices the author always inspects sample boards before and after component placement to make sure excess paste displacement has not occurred. This makes sure wet paste shorts do not occur, which can lead to solder shorts or solder beads. It also makes sure flow paths in the paste still exist and the paste is not pushed on to the solder mask around through vias if used



The two images show a single pad which has been printed with paste before and after placement of a component. This easily illustrates the impact of paste displacement on size of the deposit. The example is not provided as a bad or defective deposit, it does demonstrate what can happen when there is more displacement than necessary

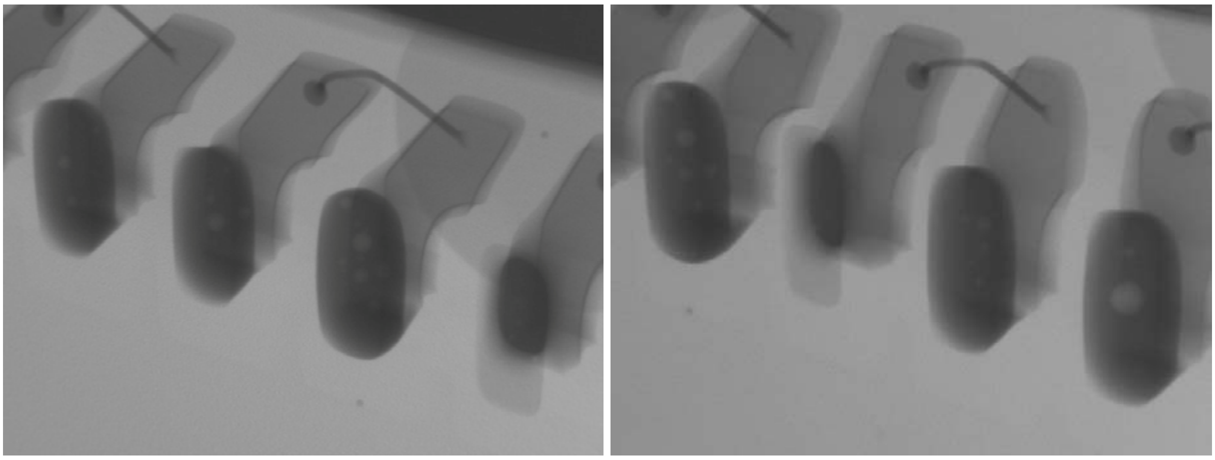
Satisfactory Paste Rework Print



In the case of QFN components it is best practice to print solder paste on to the component during rework and easier than trying to print the board for standard rework. It is also possible to print or dispense the component with paste and then reflow to bump the devices. A flux gel is then used to reflow the parts, this gives far less voiding in the joints after reflowing

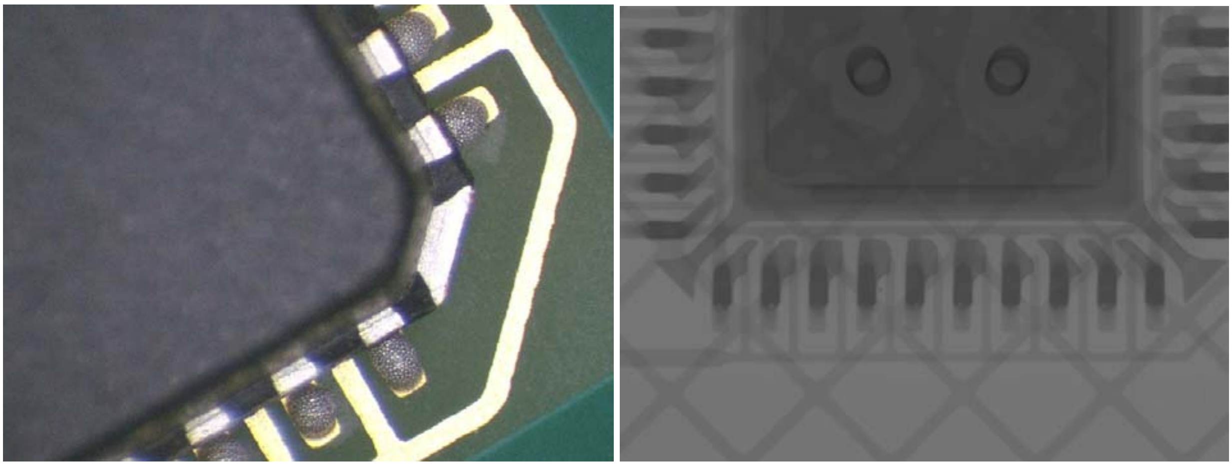
The solder paste deposits in both cases are satisfactory, however, the left image shows better printing and more control of the paste volume

Open Solder Joints



X-rays images both show satisfactory reflow of the solder paste to form joints. In both cases there is evidence of poor paste transfer on one joint per image resulting in a significantly smaller joint between the component and the PCB as indicated by the red arrows

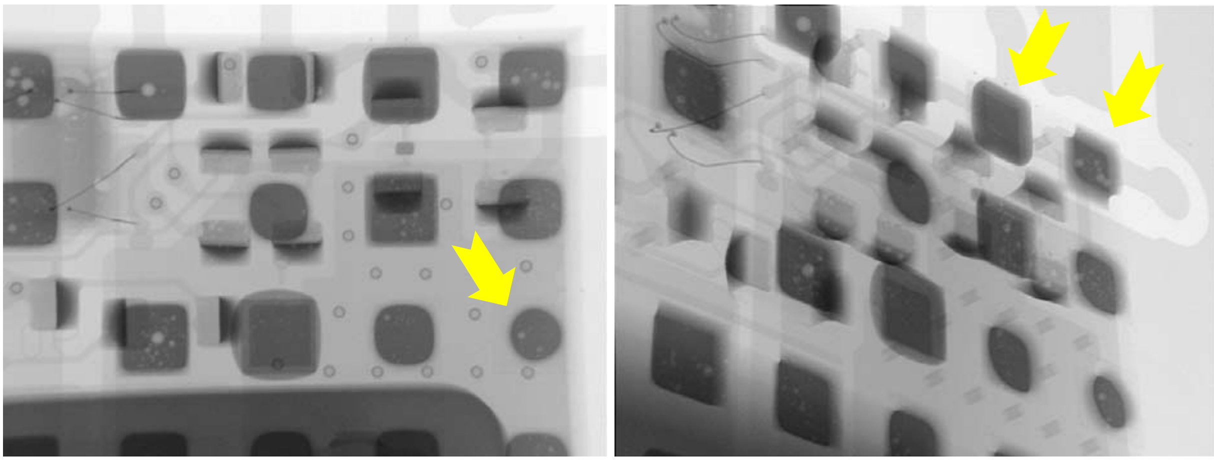
Satisfactory Paste, Place & Reflow for SIR Testing Paste



QFN package placed and reflow successfully as shown by the optical and x-ray image. In this case the paste was jetted with a My600 system on the outer connections and the centre pad. The My600 was used to assemble this Surface Insulation Resistance (SIR) test pad with special pattern under the QFN to assess cleanliness before and after cleaning. As the SIR circuit pattern needed to pass between each pad without solder mask the jetting system allowed maximum flexibility to change paste volume rather than changing stencils

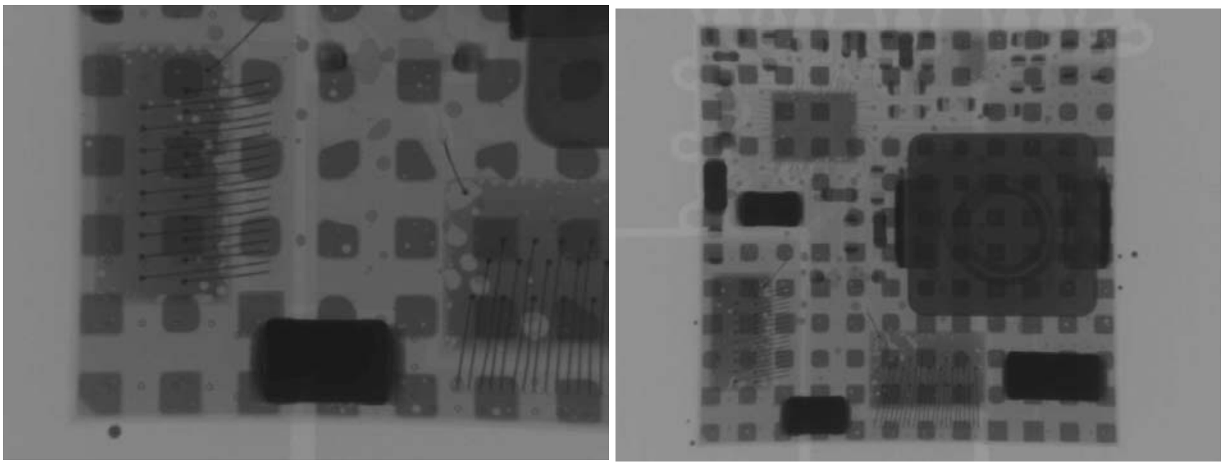
Having the SIR pattern exposed and under the device allowed the impact of different moisture levels on the surface of the board and under the package. At high humidity dendrites formed on the surface of the board; coating the board improved the performance of the test boards, even with heavy condensation on to the boards

Inconsistent Solder Joint Volume



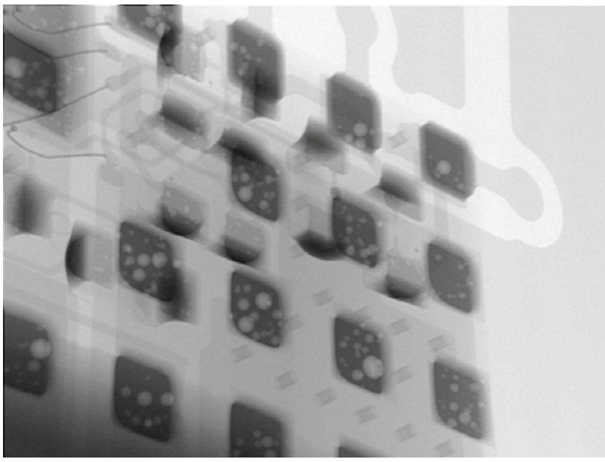
Very inconsistent solder joint volume caused by poor volume control of the solder paste printing. Looking at the examples highlighted it is easy to spot the differences in the joints. Some of the joints are even open as indicated by other defects in this guide. The pads are reasonably large so printing problems and paste transfer should not be an issue on a well-defined process. Just poor printer set-up and no post printing inspection, if you don't use automated SPI you need to use the old-fashioned way, use your eyes. I do recommend correct set-up and a test board with plastic film overlay. It means that when you start printing you know you are correctly set up and you don't contaminate boards while you get it right

Inconsistent Solder Volume & Squeeze Out



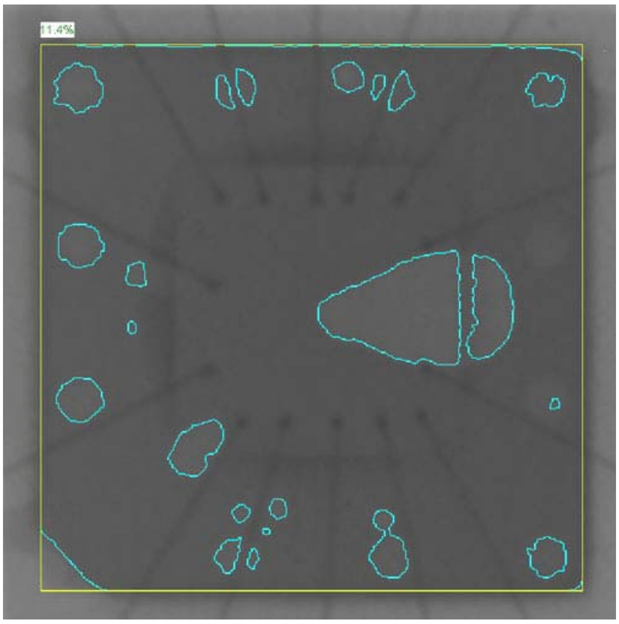
Excessive solder balls and solder beads under and to the side of the packages are created with poor control of placement force displacing the paste before reflowing. It is possible with the x-ray images to see examples of solder compressed between terminations. Solder balls can be created with the incorrect profile but under a large mass part reflow is generally slow rather than fast, so less likely to cause balling

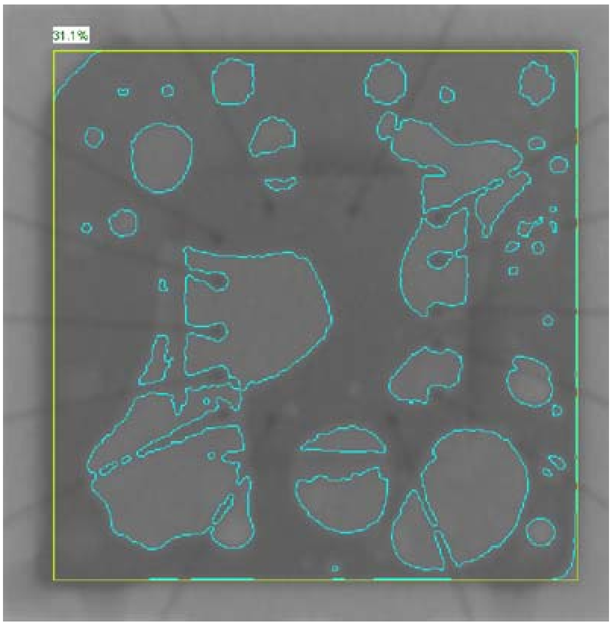
Solder Joint Voids



The number of voids in these joints is not ideal but is unlikely to impact the reliability or heat dissipation. Voids in this type of BTC package are not uncommon due to the recess of the solder mask created by the mask defined pads on the component body. Some users have bumped the parts first or had solder balls added to the packages prior to assembly to aid stand off and reduce voiding

Solder Joint Void Size





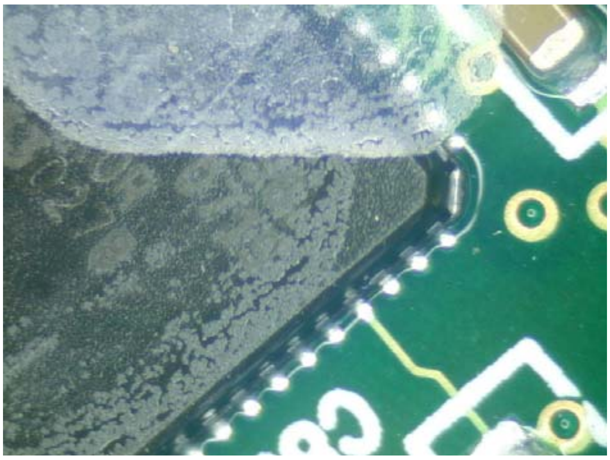
Void measurement has been conducted on two devices, the centre pad on the device on the left show 11.4% and the second image on the right 31.1% taken from the x-ray system software. Most x-ray systems offer this function in their software capability

Testing Filled & Plated Vias

Using filled and plated over via holes is possible where the pad is to be used for solder paste print and reflow. This is of course provided the stencil design, paste and the reflow profile have been well defined to reduce the void formation. However, make sure the PCB manufacturing process or the materials used do not let you down with outgassing from the surface of the pad. The choice of via filling and capping process should be discussed with the PCB supplier but also tested for outgassing during reflow

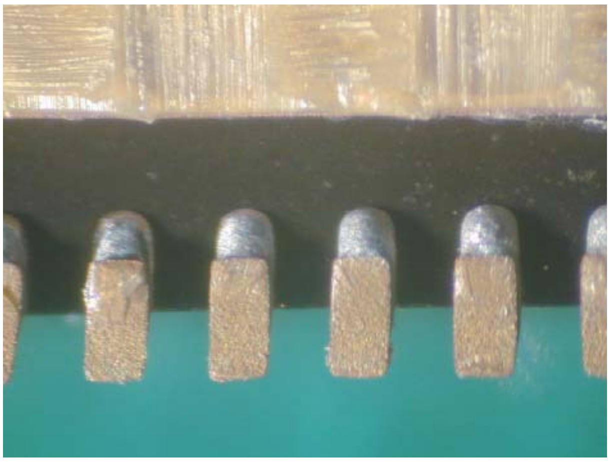
Experience has shown that all may look good but outgassing can still occur. The simplest test is to place high temperature clear oil on the surface of the pad. Then simulate the reflow profile while watching the surface of the pad. There should be no evidence of bubbles, if there is who said always blame the paste and profile?

Poor Conformal Coating Adhesion



Conformal coating to plastic parts can be an issue and is not an uncommon problem with BGA, QFP and any plastic body. It is important to confirm the problem is with the component type before the assembly process; it is possible that the assembly process may have contributed to the problem. In this case the components from the same batch showed poor adhesion prior to assembly. The only way to improve the products was to clean the assemblies, dry the board and coat. There are other pre-treatment operations prior to coating which should be discussed with your coating supplier

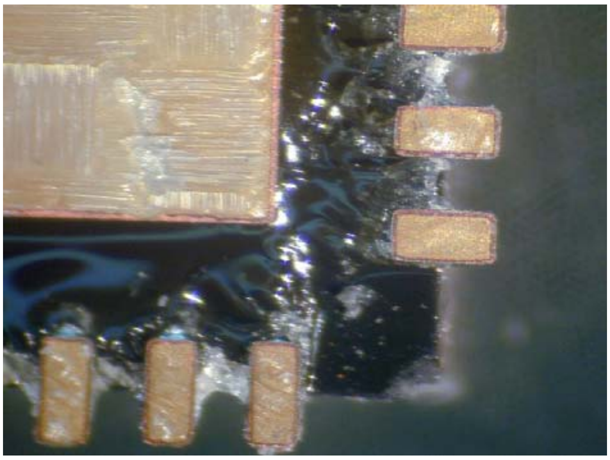
Satisfactory Cleaning Under QFN

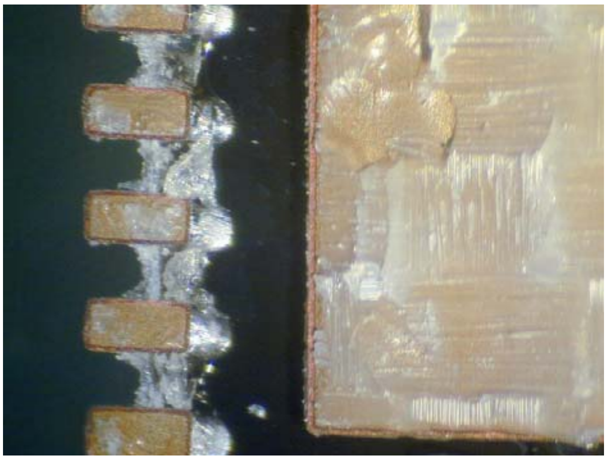


The package has been mechanically removed from the surface of the board, all the pads have separated from the surface of the board with no flux residues present on the board or package. The cleaning process used has been able to remove the flux showing that the correct combination of paste, cleaner and process parameters were used. It is possible to use ion chromatography on the board and the component to check for residues. Equally surface insulation resistance can be used to assess the reliability of the product.

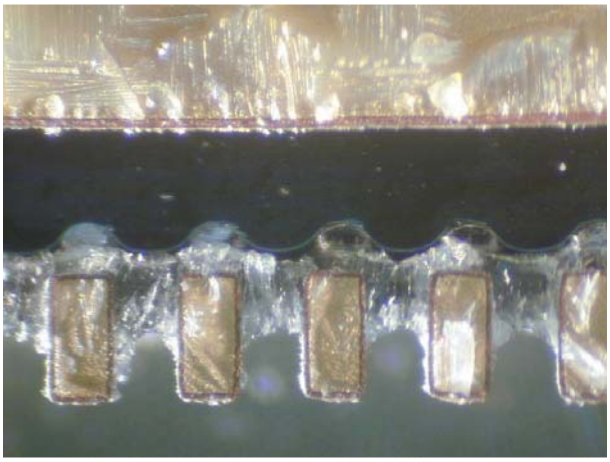
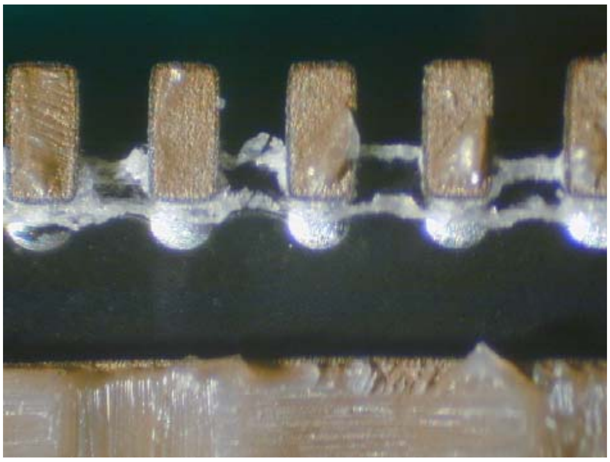
The author normally uses test boards with glass slides first in any process assessment as its simple and less time consuming before conducting more expensive but more quantifiable methods like SIR. SIR is the best method to show the potential for failure in a harsh operating environment

No Clean Flux Residue



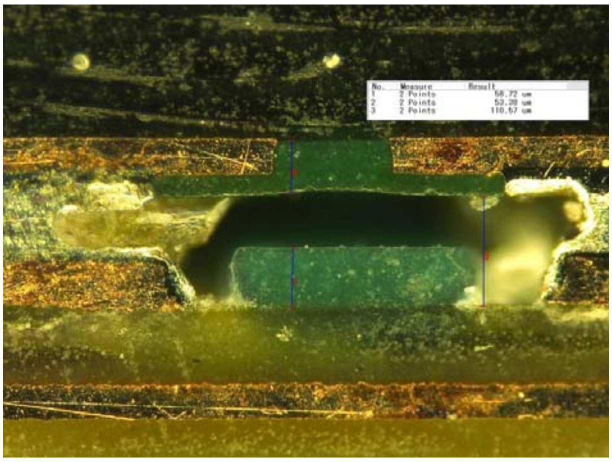


The images show QFN packages that have been reflow soldered to boards then mechanically removed to examine the flux residues under the body of the component and the terminations. There have been many debates on the effective cleaning under this low standoff package. It is clear in these examples that flux residues remain and have in some case not been removed

Experience shows that with the correct selection of paste reflow profile flux residues let can be cleaned. If the combination of flux residues is not assessed with the correct cleaner and cleaning process this is the type of result to be expected and shown above. The images show a combination of unsuccessful cleaning, practical solubility and white residues where not soluble in the cleaning process and remain

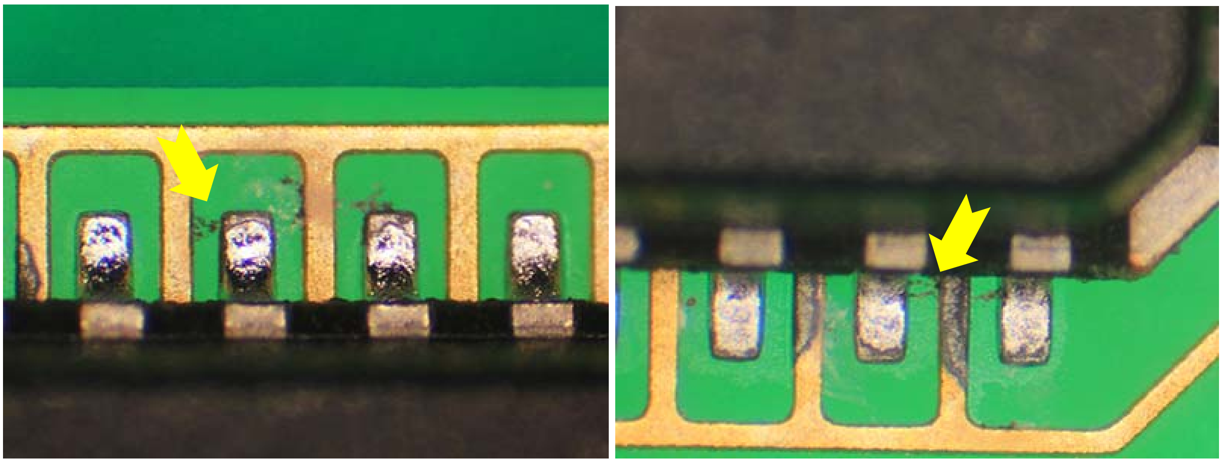
Stand Off Height Measurement



This type of package can be difficult to clean unless the process and materials are well defined and correct evaluation methods are undertaken. Just testing a board for cleanliness will not show all, but only part of the story. Its not just the standoff heights under the package but also the size of the gaps to allow cleaning solution penetration then rinse water to flow to complete the process before blowing out and drying. During the design of the board and initial NPI consider the removal of solder mask on the substrate, as you can see from the microsection resist will impact the cleaning and drying process. It is perfectly possible on many designs to remove solder mask between outer connections and between the outer contact and the centre pad making effective cleaning simpler and faster

The standoff height of this type of package also has an impact on the solder joint reliability on larger QFN parts. This is particularly true where a large die is used in small packages, a growing problem in the industry

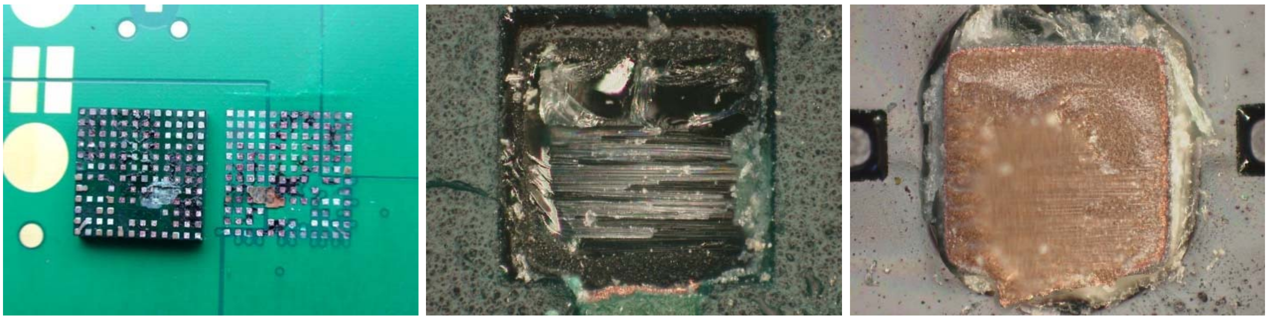
Dendrite Formation



Examples of copper dendrites formed on SIR test patterns used to measure change in insulation resistance on boards or under components. This type of assessment is used to confirm the long-term reliability of a board assembly, the type of no clean flux used or the effectiveness of cleaning. The samples shown were reflowed then exposed to high temperature and humidity. The dendrite formation is indicated by the arrows and only seen on these test samples on the edge of the package.

Further details and some video examples on SIR testing are featured on YouTube using the following Video Link

Successful Dye & Pry Testing



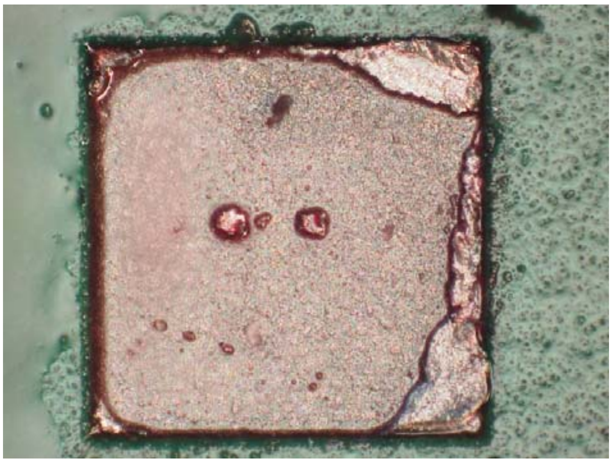
Dye and pry is a very simple and useful technique for identifying points of failure or to determine the success of soldering BGA, QFN and other area array packages. It has been used for many years by the author on customer projects. Basically, a red dye helps to identify any damage, cracks or separation between solder joints, mounting pads, laminate or surface finish on components or PCBs. A red dye can capillary around area array joints and fill cracks or voids and leave a permanent record of the fault. A package is them mechanically separated from the board after cleaning excess dye from the board and around joints. The presence of the red ink indicates the points of failure before the parts have been forced from the board

The three photographs from left to right show, the BTC removed from the board, a close up of the laminate surface where one pad has been lifted. The last image right, shows the bottom of the copper pad on a solder connection. In both cases there is no evidence of the red dye on the copper pad or in the surface of the laminate. This shows that the surfaces were still well bonded before force was applied

Practically speaking BGAs are easy to mechanically remove where as standard LGA/QFN/BTC parts are far more demanding to pry or pull from the board surface unless very poorly assembled A new test standard created by IPC is available from their website www.ipc.org

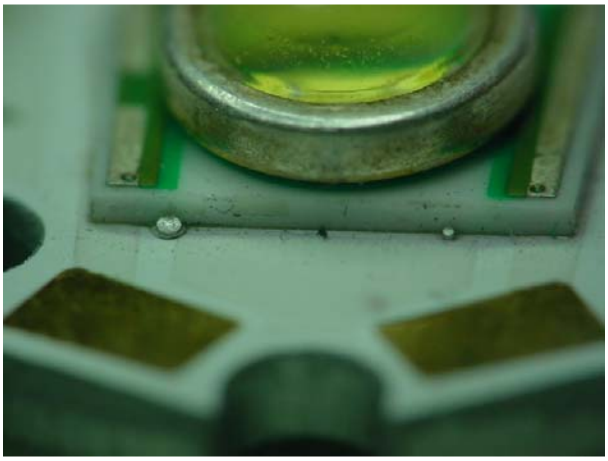
Further details and some video examples on dye and pry testing are featured on YouTube using the following [Video Link]

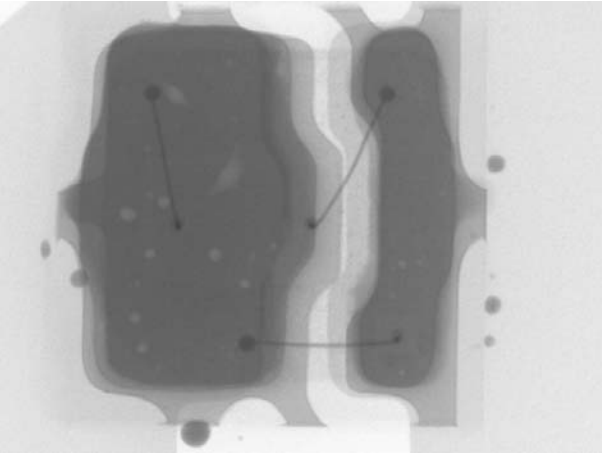
Poor Shear Result



The square pad shows limited wetting to the nickel surface after the solder paste had reflowed on the gold pad. You can see that solder has wetted to the edge of the pad like round pads on BGA packages with similar solder joint separation. Close examination of the surface of the pad showed no solder wetting or intermetallic formation. Only the gold had been consumed during reflow by the lead-free solder paste. Microsections of other parts showed some evidence of wetting to the pad but not complete. Joints on the device were known to be intermittent during test and the shear force when measured was also lower than would be expected. The problem was seen on other parts of the board and resolved with better control of the nickel plating bath at the PCB supplier

Solder Balls & Beads





Solder balls or beads have been around since the start of SMT, basically the solder balls around the edge of devices are normally referred to as beads. The reason is to avoid confusion between random solder balls on other parts of the board. Solder beads in these optical and x-ray images are caused by excess solder paste printed on the substrate. When solder paste reflows and it is not in contact with a solderable surface to wet on the part or substrate it is squeezed out to the side of the part as shown

During assembly, the stencil design should be optimised to suit the component, the placement force applied to the component examined and the substrate design rules reviewed. Do not just copy the component supplier's recommendations, use your knowledge and experience. Although many customers report the beads are seen with a change in paste which is understandable if the process was not optimised for the new paste. Often this is not considered when changing from paste to paste

Video examples of solder beading are featured on YouTube Video site using the Video Link

QFN/LGA Reference Books & Standards

The following documents are available to purchase from publishers and distributors. As a book reviewer, the author has covered many of the titles in his book review videos available to watch online via YouTube follow the link provided Here

IPC - 7093 Design & Assembly Process Implementation for Bottom Termination Components
IPC – 610 Acceptability of Electronic Assemblies
Chip Scale Package – McGraw Hill
Wafer Level Chip Scale Package – Springer
LED Packaging for Lighting Applications – Wiley

PCB Surface Finishes & Solderability Standards & Text Books

IPC-4552 Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards
IPC-4553 Specification for Immersion Silver Plating for Printed Boards
IPC-4554 Specification for Immersion Tin Plating for Printed Circuit Boards
IPC-4555 Specification for Organic Solderability Preservative (OSP) for Printed Circuit Boards (Committee Draft)
IPC-4556 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) Plating for Printed Circuit Boards

IPC J-STD 003 Solderability Tests for Printed Boards
IPC 600 Acceptability of Printed Circuit Boards
IPC 610 Acceptability of Electronic Assemblies

In addition, a specification for solder levelled boards is required as well as other new finishes

The following are text books on printed board manufacture which include details on surface finish

Printed Circuit Handbook (7th Edition and the PCB Manufacturing Bible)
Clyde Coombs, Jr. - McGraw Hill

Flexible Circuit Technology 4th Edition
Joe Fjelstad – BRP (Free Download)

Comprehensive Guide to Design, Manufacture of Printed Board Assemblies
Bill MacLeod Ross - Electrochemical Publications (Finishing Publications Limited)

Quality Assessment of Printed Circuit Boards (Out of Print search on-line its worth it)
Preben Lund - Bishop Graphics Inc.

SMT for PC Board Design (2nd - 3rd Edition)
James Hollomon - Prompt Publications

PCB Training Material & Services

Over the last few years we have created several products and services for education which are commercially available worldwide. These products and services are based on practical experience and evaluation projects conducted by the author. Any of these products or services can be obtained online www.smartgroup.org or in the case of CD-ROM and poster sets they can be obtained from other industry groups like IPC and SMTA www.smta.org We do provide onsite training and online webinars on all aspects of QFN/LGA and BTC defect prevention for details technical@smartgroup.org

PCB CD training products, photo CD and sets of inspection charts shown above can be obtained from the following organisations or websites

SMART Surface Mount & Related Technologies Association
www.smartgroup.org

SMTA Surface Mount Technology Association
www.smta.org

IPC
www.ipc.org

For further information on products or to book a workshop or webinar contact www.smartgroup.org

Workshops/Webinars on QFN Design, Assembly, Rework & Inspection

The length or the delivery method of training can be adapted to suit your team and location and needs. The course content can also be changed to suit your company requirements

QFN/LGA/BTC Design & Assembly Process Implementation

QFN/LGA/BTC Inspection & Defects – Causes and Cures

QFN/LGA/BTC Rework & Repair Methods

QFN/LGA/BTC Cleaning Process Optimisation & Assessment Methods





Author's Profile

Bob Willis currently operates a training and consultancy business based in UK and has created one of the largest collections of training material in the industry. He is a member of the SMART Group Technical Committee. Over the years Bob has been Chairman and Technical Director of the SMART Group and holds the title of Honorary Life Vice President for his contributions to the Group since its inception. With his online training webinars Bob Willis provides a cost-effective solution to training worldwide and regularly runs training for SMTA, SMART, IPC and recently EIPC. Although a specialist for companies implementing lead-free manufacture Bob has provided worldwide consultancy in most areas of electronic manufacture over the last 30 years. Bob has travelled in the United States, Japan, China, Malaysia, Russia, New Zealand, Australia, South Africa and Far East consulting and lecturing on electronic assembly

Bob was presented with the ***"Paul Eisler award by the IMF (Institute of Metal Finishing)"*** for the best technical paper during their technical programmes. He has conducted SMT Training programs for Texas Instruments and ran Reflow & Wave Soldering Workshops in Europe for one of the largest suppliers of capital equipment. This is based on many years of practical experience working in telecommunications, military OEM, contract assembly, printed board manufacture, environmental test and quality control laboratories. This has earned him the *SOLDERTEC/Tin Technology Global Lead-Free Award* for his contribution to the industry. He has also been presented with the *SMTA International Leadership Award* and *IPC Committee Award* for contribution to their standards activity

He has also run training workshops with research groups like *ITTF, SINTEF, NPL & IVF* in Europe. Bob has organised and run lead-free production lines at international exhibitions *Productronica*, *Hanover Fair*, *Nepcon Electronics* in Germany and England plus IPC APEX and SMTA International in USA. Providing an insight to the practical use of lead-free soldering, high temperature electronics, cleaning, conformal coating on Ball Grid Array (BGA), Chip Scale Package (CSP), 0210 chip and through hole intrusive reflow connectors. In September 2016 Bob was presented with *Best Speaker at SMTA International Conference* 2016 in Chicago

He has worked with the GEC Technical Directorate as Surface Mount Co-Ordinator for both the Marconi and GEC group of companies and prior to that he was Senior Process Control Engineer with Marconi Communication Systems. Following his time with GEC he became Technical Director of an electronics contract manufacturing company where he formed a successful training and consultancy division before setting up his training and consultancy business