

Cleaning & Contamination Defect Guide

Bob Willis



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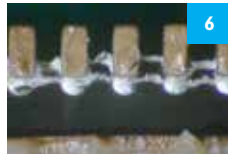
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Introduction

We hope that you find the “Cleaning & Contamination Defect Guide” a useful and informative reference for recognizing and solving problems within your manufacturing or suppliers process. The defects included in the guide are fairly common process issues or failure modes that engineers in the industry have experienced over the years.

This guide is a live document that will be updated on an ongoing basis, with the latest edition being made available in print and as an online interactive edition.

I have been involved in training, process development and disseminating information regarding printed board manufacture and assembly for many years.

I have had the pleasure of writing for *Global SMT* magazine since the first issue. It’s a pleasure to launch this publication at the first NPL/IPC Cleaning and Contamination Testing Center held at IPC APEX Expo.

As we in the industry have seen, the defects encountered during and after implementation of new design and, in recent years lead-free soldering have brought us a variety of new and, in some cases, old challenges. This free guide is a compilation of defects associated with clean and no clean processes designed to help managers, designers, engineers and operatives to solve these everyday problems and to let them troubleshoot effectively and efficiently.


We hope you find this a useful guide and that it helps you achieve your objective. If you find cleaning related defects not included in this first edition we would like to hear back from readers—email bob@bobwillis.co.uk.



Bob Willis

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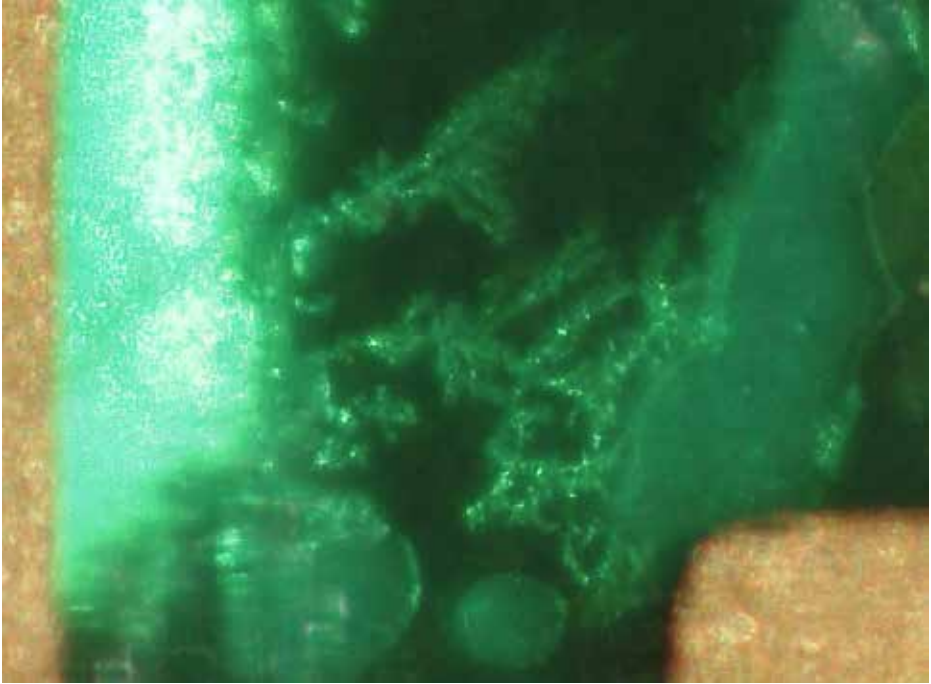
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Copper Dendrites/Surface Corrosion

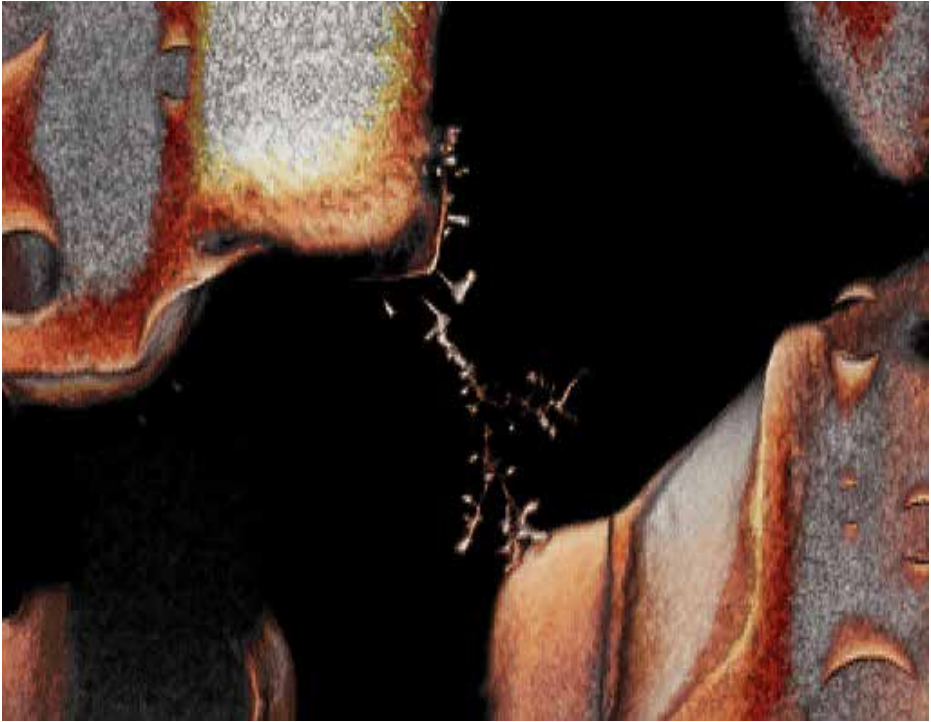


Copper dendrites, one of the most common failure modes, and three ways of seeing the same failure.

The figures here show three dramatic examples of copper dendrites formed on the surface of printed circuit board assemblies. In each case they lead to intermittent failures in the field. They are not specifically lead-free process related but can occur if the correct controls are not maintained in a manufacturing facility; some engineers have reported this failure mode in lead-free when moving to VOC free fluxes. Copper dendrite will occur with a tin/lead and lead-free process and need to be analyzed to find the root

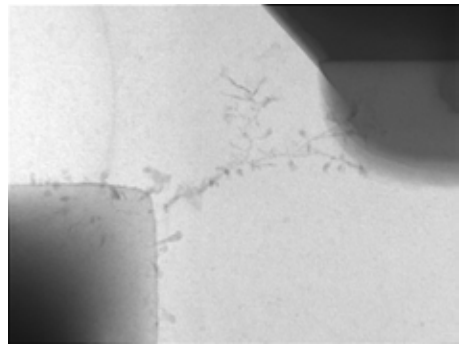
cause of the problem. The examples show the formation of a copper dendrite/fern between two conductors. This fault may occur when flux residues remain on the board surface and are then subjected to high temperature and humidity. A circuit with a voltage applied of 5-10 volts can then allow the formation of a conductive path on or through the moisture layer.

A copper dendrite often creates an intermittent fault which can be very difficult to pinpoint. Examples like these can be seen under and over solder mask coating or under conformal coating when there is poor surface adhesion of the coating hence the contamination on basic printed board is important. Contamination testing and Surface Insulation Resistance



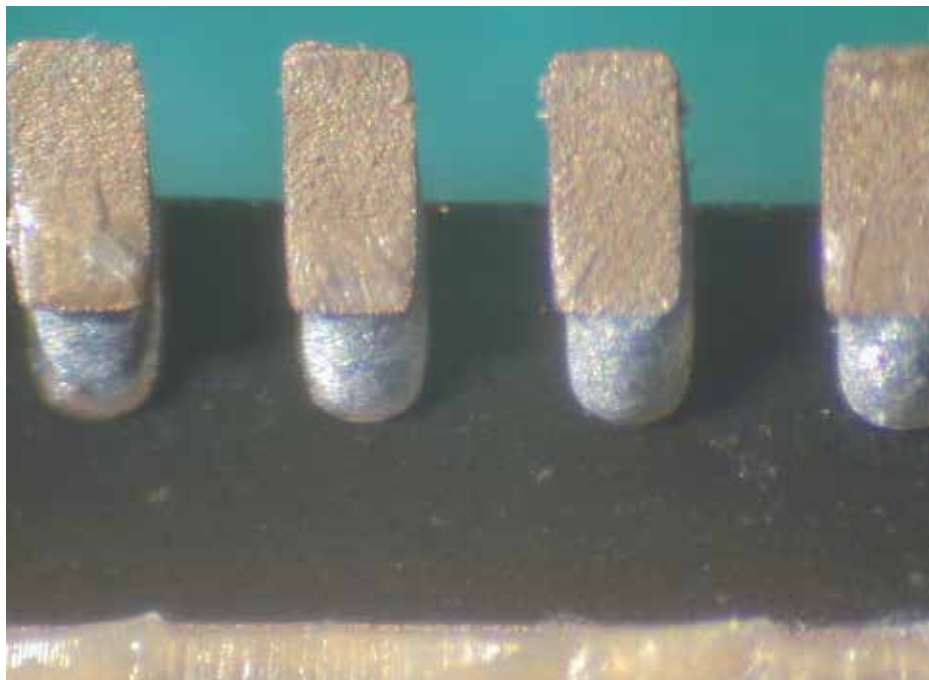
(SIR) assessment are two techniques often used to monitor and control the levels of harmful contamination or assess the assembly materials performance on finished products to help avoid the possibility of corrosion.

Contamination that causes this failure mode is not only from the flux, it can come from the level of cleanliness of the printed board prior to use. It can also be caused by the design of the board, the way it is mounted in a product and exposure to changes in temperature and humidity. Three different techniques were used to investigate the failure shown above. The image on the previous page shows back grinding a microsection up under the chip component to avoid removing the evidence of failure as so often happens in test department. Standard high resolution



x-ray was used in the second example after the location of the product failure had been established. This technique was used to examine for failure in similar locations on other products. Using x-ray with CT capability allowed a three dimensional view and a clear understanding of the position of the dendrites without sectioning.

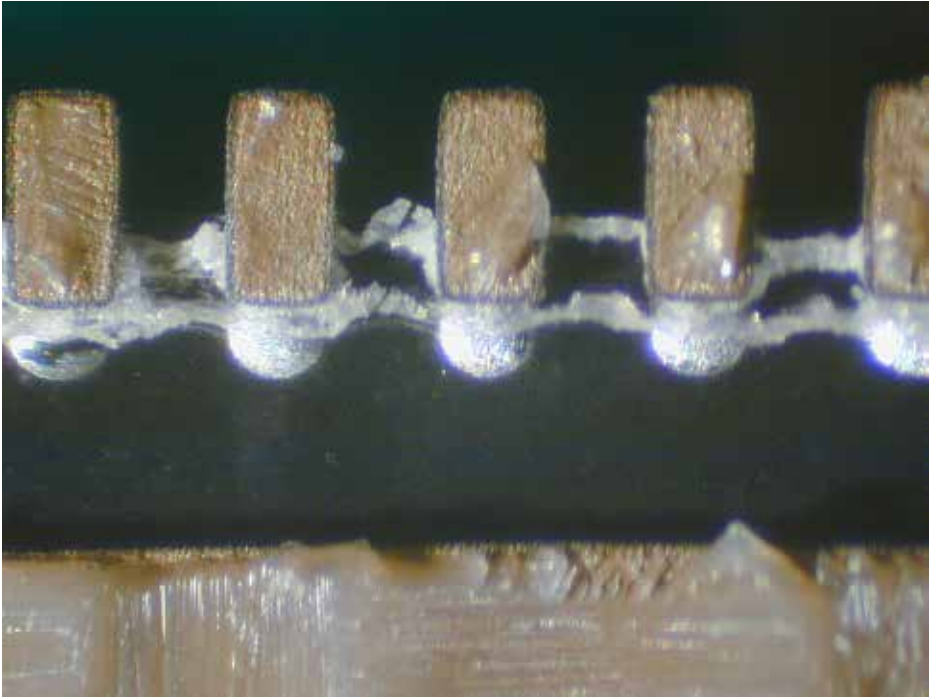
Cleaning Under QFN



Successful cleaning under low stand-off height QFN packages can be achieved as shown on the above image; poor flux and cleaner compatibility is shown on the image on the next page. Both were cleaned in a batch process using different process recipes. The sample parts were removed from the surface of the board mechanically to show the process performance.

Modification to the design rules for a component can also increase the reliability of the cleaning process and, if marginal, also reduce the risk of failure. Increasing the distance between the termination pad and center pad, elimination solder mask under the package can also help cleaning performance.

Cleaning Under QFN (cont'd)



The key to evaluating residue removal is the solubility of the residue in the cleaning material before undertaking the actual cleaning trials. When this is established then the correct cleaning process

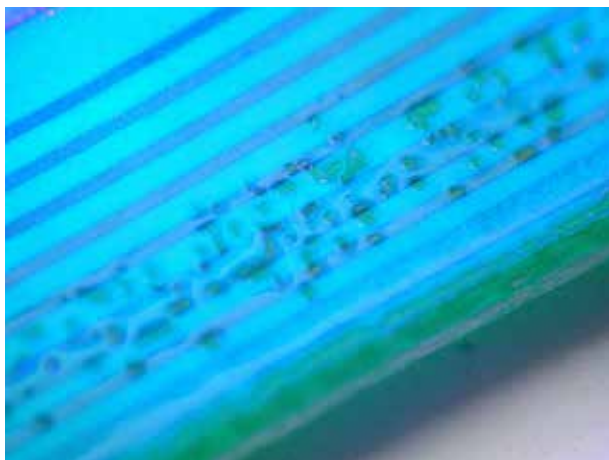
can be defined to allow full penetration under the components of the cleaning chemistry before confirming that it can also be removed during the rinsing phase of the process.

Mask De-wetting or Poor Adhesion

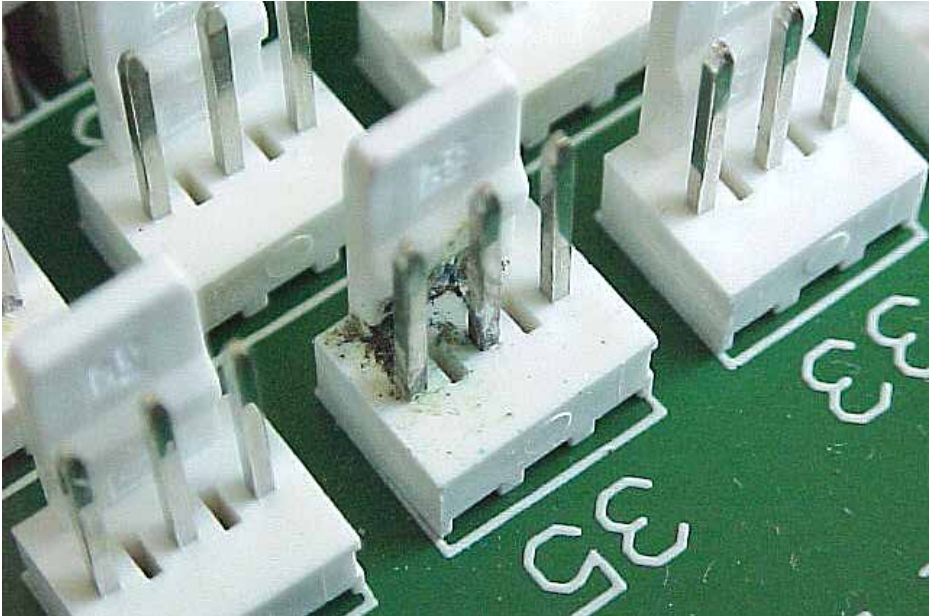
Both defects shown at right can be the result of poor cleaning process design or incompatibility of the surfaces being coated. In the first case it's questionable if the dewetting will have any impact on the reliability but its better to solve the problem on future products. The top image shows conformal coating has separated from the surface of a plastic QFN/LGA body which is not uncommon on many plastic parts. Devices often have release agents on the surface which make coating adhesion difficult to maintain, minor loss or separation may not normally be reworked. In this case the root cause should be established as all the coating has completely lifted.

Cleaning the board assembly after soldering may overcome the problem in future production runs but equally it may not. The

fault can be seen on most coating systems, more likely on thinner coating, although the poor adhesion will still be apparent on thicker coating but may not be easily displaced. The bottom image shows dewetting on the surface of the solder mask above a series of copper tracks on the board. As this was apparent on the edge of the board it could be due to handling either at assembly or during board fabrication. If the solder mask coating on the board is sound it's not likely that the minor dewetting of the conformal coating in this area will affect the product's reliability; however most customers would not accept a product in this condition.

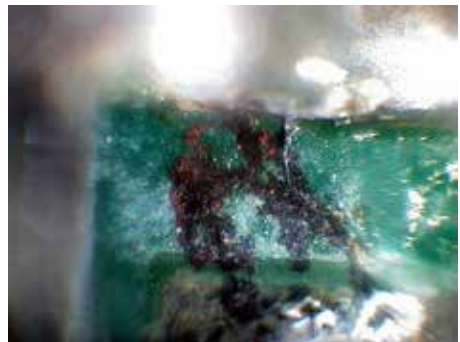


Corrosion Dendrite Formation



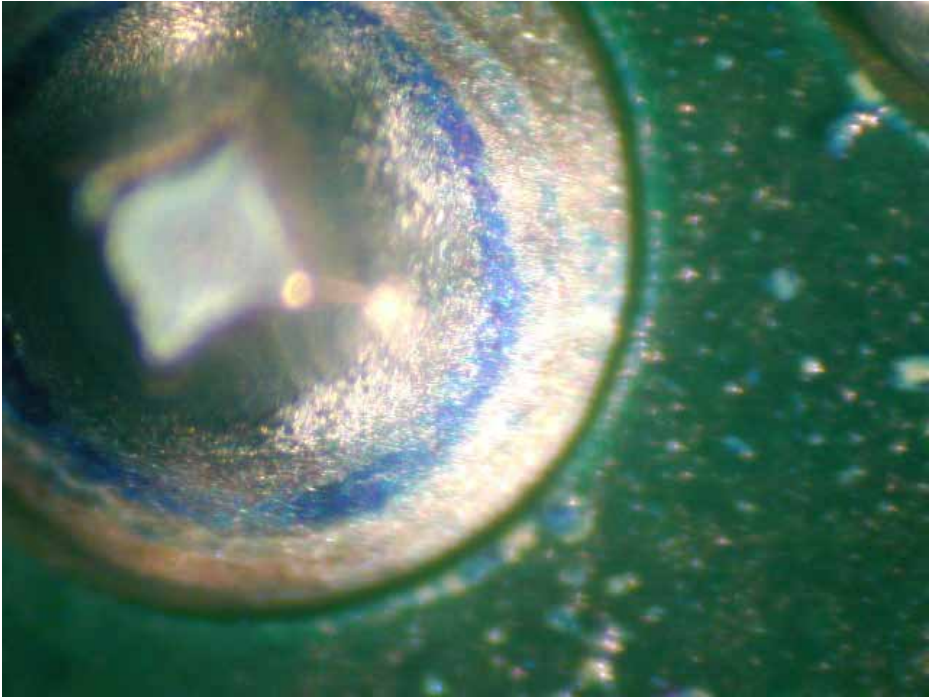
Corrosion and dendrites have formed across the surface of the plastic connector body between two terminations in the above photo. This was caused by excessive flux being sprayed on to the top surface of the board. The flux could have also penetrated up through the connector by capillary action between the pin and connector body.

In the case of no clean materials, they need to be exposed to the correct preheat to allow full evaporation of the carrier solvent and deactivation of the flux. If a conformal coating had been used in this application the same problem could have occurred on other sections of the board. Coating cannot overcome poor production set-up or control when potentially corrosive materials are still on the surface of the board. The smaller image shows



copper dendrites between two connector terminations. The copper has formed over the solder mask due to the high concentration of moisture on this area of the circuit. This demonstrates that solder mask does not always help!

Flux Residue Testing



This is not contamination on the surface of the through hole joint; it's the result of testing board surfaces for different contamination types. Traditionally contamination on the surface of a board assembly is tested using an ionic contamination measuring system, Surface Insulation Resistance (SIR) or optical assessment which is explained in many of the IPC standards. Two simple fluid test indicator systems are available; they test for flux activators or resin on the surface of joints either before or after a cleaning operation and prior to coating.

Basically the test fluid is placed on sample areas of the board assembly or on selected joints. The fluid must be left on the surface of the test feature for a fixed

period of time for a reaction to take place. There are two different fluids, one for activators and resin systems. In the example a through hole termination produced by selective soldering has been tested for flux activators. The change in color shows a positive result indicating there are activators still present on the solder joint surface. Residues can also be seen around the joint on the solder mask. A company would need to establish their own criteria between this test method, cleanliness results, SIR reliability data and possibly product exposure to specific operating environments.

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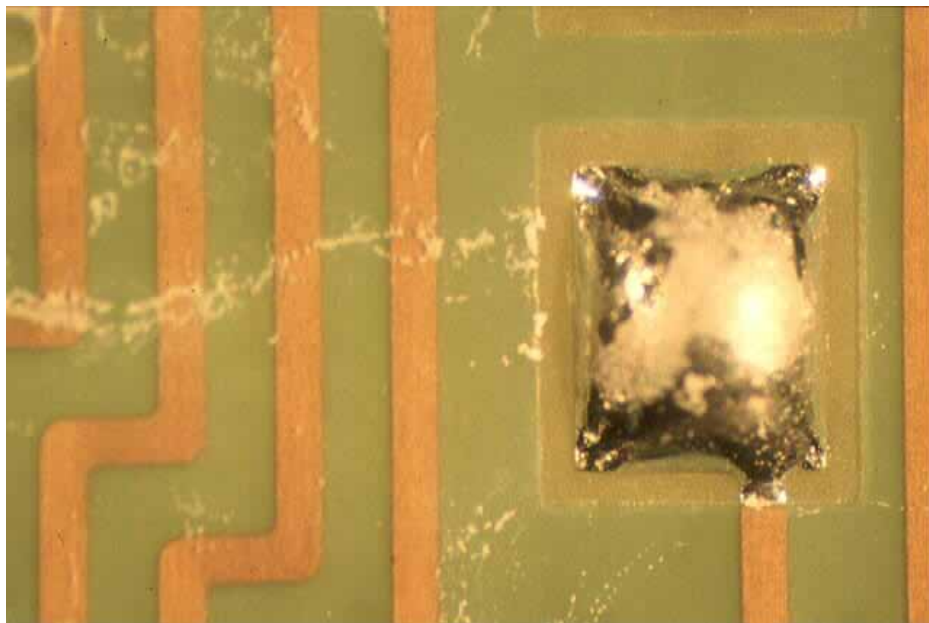
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No Clean Flux Residues



Flux residues visible on the board surface are more common due to the significant use of no clean processing. However, in a well-engineered process with the correct selection of flux, solder mask and process conditions the surface of a board after wave or selective soldering can be visually clean. The reliability of no clean materials has being demonstrated over many years in automotive and medical products through good process engineering.

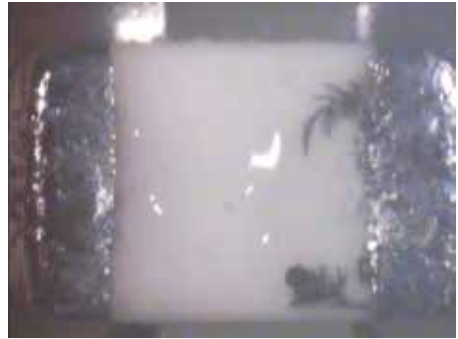
In the example shown above, the residues are either as a result of the formulation of the flux or due to poor process conditions. Many no clean materials rely on the correct pre-heat temperature helping to minimize the residues left on the top and bottom of the board. Wave contact time and temperature also affects the residues left on the board. Discussion

with the flux supplier should provide the correct process parameters but never forget to control your PCB suppliers, solder mask changes and monitor your flux application process for the quantity of material being applied.

Dendrites/Surface Corrosion

At right is a sequence of images captured from a video of dendrite formation. It shows in real time the slow growth of dendrites between two terminations on a chip component with a voltage applied to the terminations. This is a simulation on what can occur under a component if the incorrect flux is used in production. This is a simple test method used by a flux supplier to evaluate rework flux in a close to production environment. It's also a particularly useful way of showing the significance of using the right materials to production staff and the consequence of not using approved suppliers and process conditions. The most common form of dendrites found on the surface of printed board assemblies is copper; however this can be other forms of fern growth based on the termination plating.

The speed of dendrite formation would be dependent on the material, voltage applied and separation distance between terminations. This is also the case in a normal failure but is also exaggerated by the level of surface moisture.



Dross or Oxide Short



A solder whisker or a dross short is surface contamination that can be found after soldering due to either a poorly maintained solder bath or incorrectly setting of a wave. If a solder bath is poorly maintained, dross can be present in the ducting below the solder surface. When the wave operates any dross can emerge randomly in the wave and contact the board and form micro shorts.

In the case of the back flow on a lambda style wave the solder should flow at the same speed as the board or slightly faster. The board displaces any surface oxides on the surface of the wave before it can contact the base of the board. If the wave stops flowing before the board exits the wave the board will contact the surface oxide leading to what is sometimes referred to as snail trails. This can also be

seen on waves running nitrogen where only the surrounding areas of the wave are inserted.

Similar micro short have been seen during wave soldering in a lead free process where the level of copper is excessive and the temperature has allowed tin/copper needles to form and flow in the wave. The same is true if the surface of the tank becomes eroded allowing tin/copper/iron needles in the bath. Both these contamination issues can lead to very fine needle like solder shorts. The excess copper can be overcome with balancing out the copper levels with tin. The tin/copper/iron is a real problem to the system but also the extremely expensive alloy which will need to be changed.

Stranded Wire Corrosion

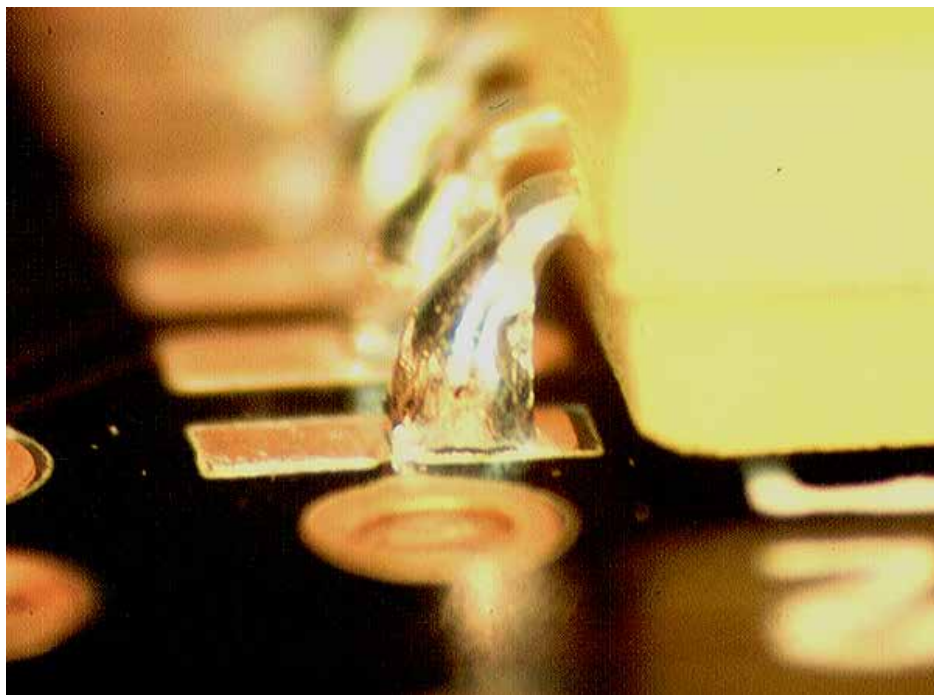


It is poor practice to use activate fluxes when tinning or soldering wire terminations to printed boards or connectors due to the difficulty in cleaning residues. If residues penetrate or are trapped in the wire and insulation interface corrosion may occur and ultimately the wire will break as the example shown at right.

It is even more of a problem to use activated material on very small wires or stranded cables due to the possibility of corrosion. In the case of stranded cable the flux will capillary along the strands of

the wire or be pushed ahead of the solder as it wets the stranded cable. Very thin wires can also be fully dissolved by solder and not necessarily the flux and has been seen during lead-free assembly due to the high dissolution rates of selected alloys.

Solder Wicking

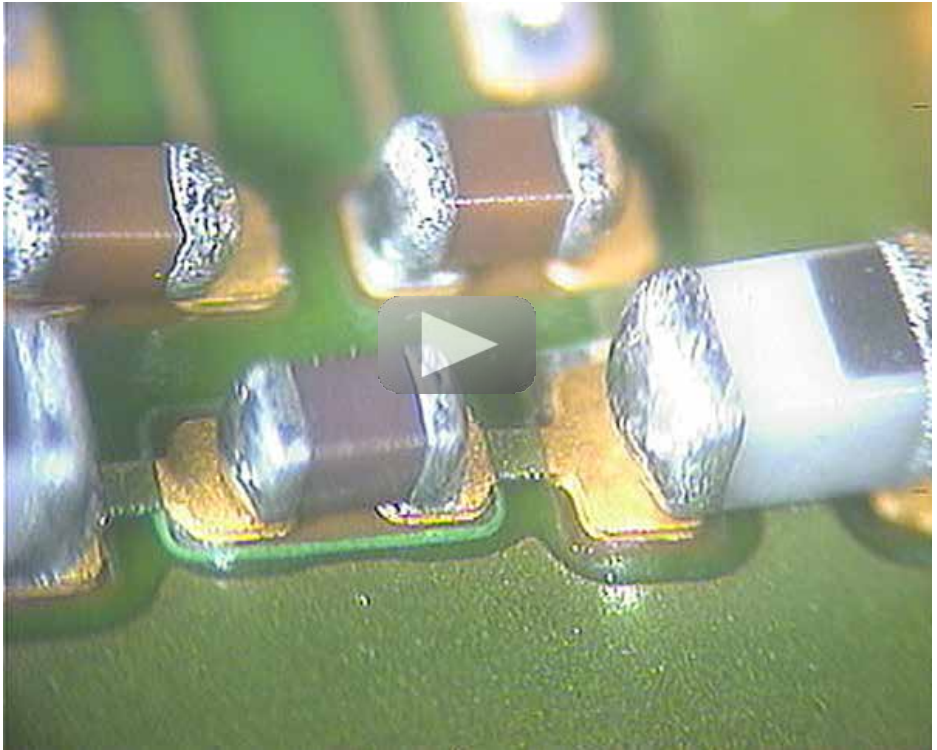


The images on these two pages show classic examples of solder wicking where the solder has all reflowed and wicked up the component terminations. In these cases it is clearly the fault of the printed board solderability.

However, don't be too quick to blame the PCB supplier; it may be an assembly

problem. Copper surface coating can be degraded by washing the board; storage times in excess of six months and high cure or reflow temperature. Make sure you confirm the true cause of the problem. In this first case (above), it is cleaning of the copper OSP board.

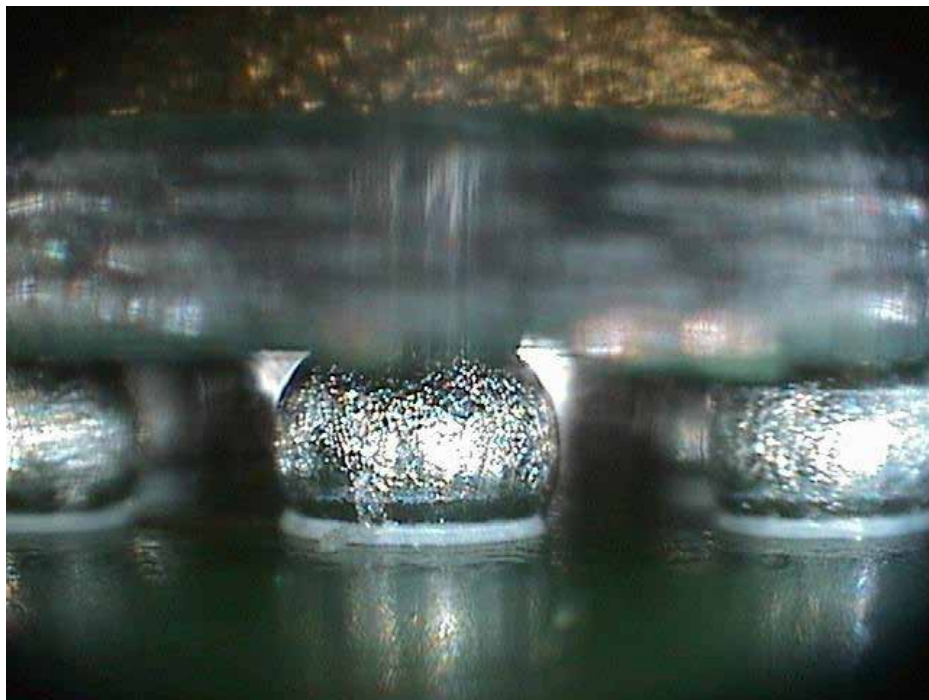
Solder Wicking (cont'd)



In this image, the wicking on the gold pads was caused by poor cleaning on the surface of the board prior to reprinting and reflow. Poor control or selection of a paste wash off process for poorly printed solder paste can result in this type

of defect. It's much better to spend time setting up the printing process correctly than the possibility of unknown surface contamination.

White Residues



White residues are normally associated with flux residues that have not been successfully removed from the surface of a board assembly during a cleaning process. The most common reason for this is the incorrect combination of flux and cleaning materials being used. It's very important that the combination of materials is fully evaluated during the process development stage. Any changes of paste, wave or rework flux are tested before they are used in production. The soldering temperature can make materials less soluble or some other process induced contamination.

The example above of BGA joints with a perfect white ring around the terminations is the same problem but in another

process. This board and others seen over the years are examples of no clean paste residues after reflow, in air or vapor phase left after contamination testing. Ionic testing uses either 75/25 or 50/50 alcohol and demineralized (DI) water as a test solution to remove any ionic residues left on the surface of the board. In this case the test solution has failed to remove the residues and detect any contamination. If any board is used for testing from a production batch it's good practice to mark the sample for future review.

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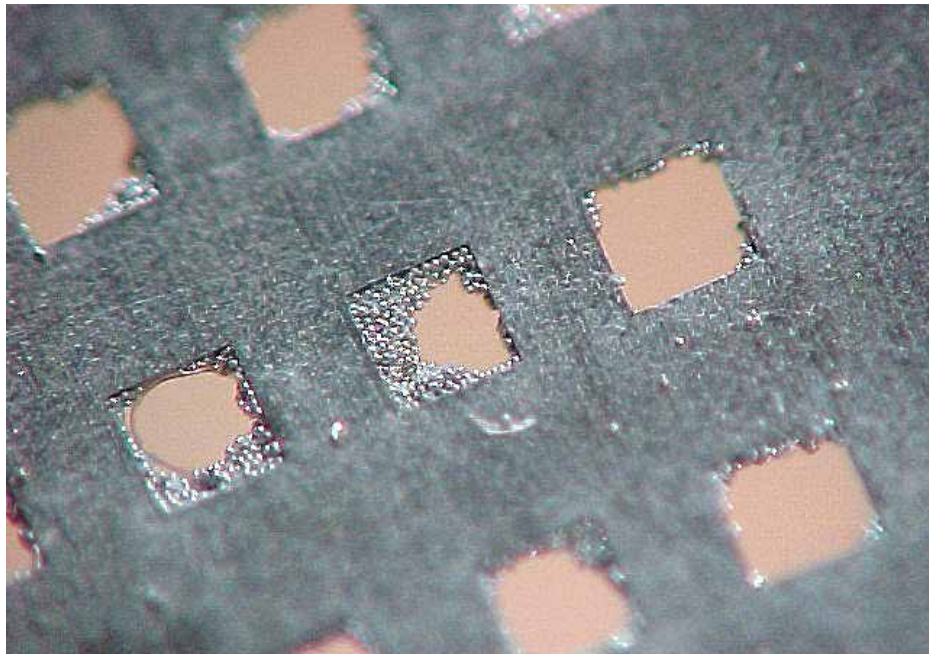
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Poor Stencil Aperture Cleaning



Properly cleaning solder paste stencils is key to success during printing, any partly blocked apertures will result in inconsistent printing. Different paste volumes normally result in ones joints on small and fine pitch terminations. Poorly cleaned apertures also lead to solder particles with nothing to hold the balls together which can result in random particles on the surface of a stencil or worst case ground into the bottom of the foil. Random paste particles can then be transferred to any boards being printed. Its great for adding unwanted solder dots to gold boards during reflow. It is surprising during process audits how often the quality and consistency of cleaning is highlighted when it can directly contribute to

different process problems. The example is not untypical of a poorly cleaned foil.

IPC have a “Stencil and Misprinted Board Cleaning Handbook” IPC 7526 which provides guidelines to cleaning, handling and inspection of stencils and provides a good introduction to improvements in stencil use and ultimately better printing. In most cases a paste supplier will give recommendations on the cleaning material most suitable for removal of paste but it’s important to check the impact, if any, on the stencil and bonding to any frame.

Pin In Hole Reflow Residues



When implementing pin in hole reflow you will use a lot more solder paste to fill a plated through hole than any surface mount joint. As the metal content is less than 50% there is a lot more flux on and surrounding through hole termination and any filled via holes after reflow. It is good practice during the design stage when this assembly process is to use test pads and not probe the through hole joints or vias.



The two examples on this page are fairly typical of reflowed joints with flux on the surface. However good the paste residues are for probing and the temperature profile is optimized residues will remain and contaminate test pins.

Component Process Compatibility



A cleaning process after soldering is chosen on the basis of the degree of cleanliness required, the type of flux residues to be removed and the accessibility of this residue to the cleaning solvent. Today the majority of assembly companies use a no-clean process but solvent in the flux can still affect parts even if it is just cosmetic. The most common cause of flux on the top side of the board is overspray of flux a process that generally goes hand in hand with no-clean processing. A combination of solvent and higher top side temperature has caused the through hole component, shown below left, on the top side of the board to deform around base. The chip resistor was damaged due to a two step cleaning process of solvent and water

wash. The parts were not degraded with a single step process

The cleaning options available are water cleaning, semi aqueous or limited solvent systems. All components must be chosen to be compatible with the cleaning process if used, rather than the process being modified to suit the components. Therefore it is important that during design and the procurement of components, compatibility with the cleaning materials or flux solvents must be confirmed. Cleaning is an area that has seen little discuss due to the wide spread use of no clean materials. Limited testing of parts is conducted for the same reasons so it's an area of concern if parts are not tested. The images on this page and the next show

Component Process Compatibility (cont'd)

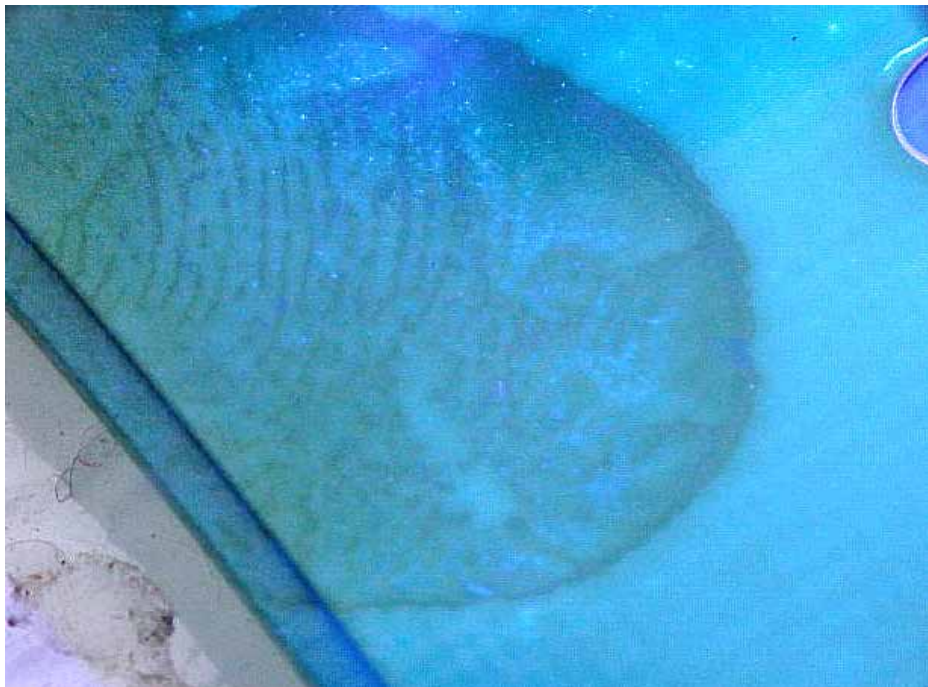


the impact of not testing parts prior to use in products.

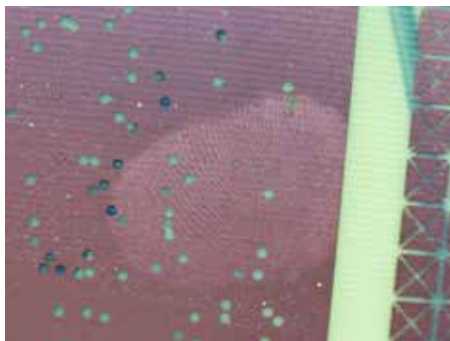
A component test program should be implemented to confirm compatibility, it is often not sufficient to just review literature from component manufacturers. Not only can some components be damaged by some cleaning processes, the interaction between the solvent and the component material can lead to increased contamination level on the final product. Certain components, such as open relay, can suffer ingress of water or contaminated solvent which is then retained within the component by surface tension forces until it evaporates, leaving the component with unwanted contamination or giving rise to potential corrosion prob-

lems. Sealed components expand during soldering, cooling during cleaning allows the possibility of material to enter the component passed the seals. The use of some two stage or semi aqueous processes have suffered from this, the first step cleaning agents can be trapped in parts and corrode the pa because the second stage generally water could not remove the cleaning agents.

Contamination and Finger Prints

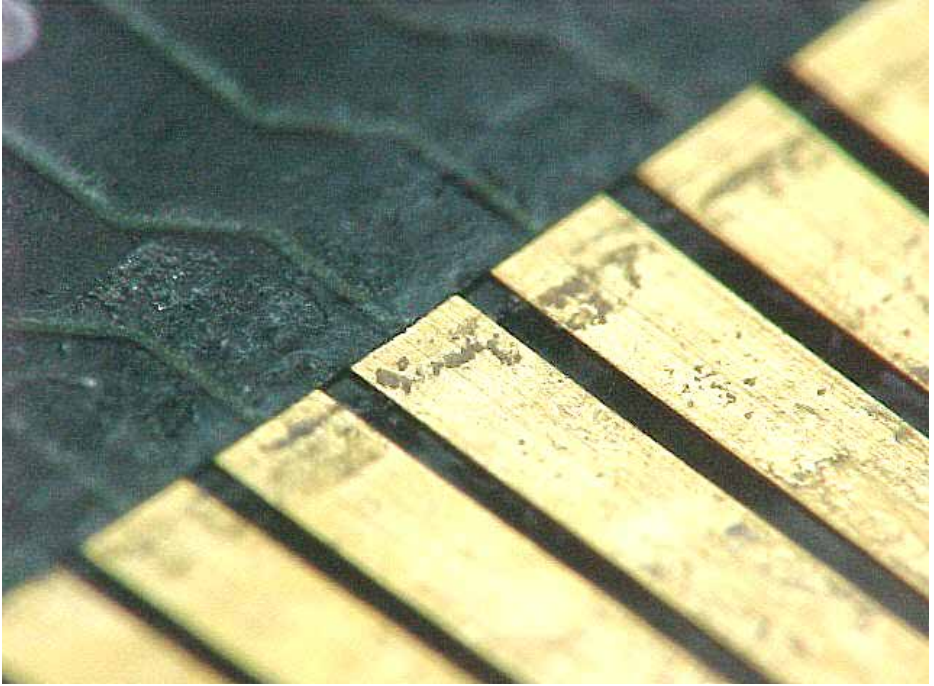


When handling bare or assembled boards they should always be held by their edges without holding the board between two fingers, thus avoiding unnecessary contact. In some industries people like to use gloves or finger bobs but careful handling can still be conducted without leaving marks or transferring contamination to the board assembly even in a conformal coating area. The image above of a finger print in a tacky conformal coating is easy to avoid. Finger prints left on the surface of the solder mask can cause dewetting on conformal coatings. Finger prints left on bare copper surfaces on PCB inner layers could easily result in poor bonding and delamination (smaller image) and can again be avoided with care.



A lot of factories do use gloves or finger bobs but they get dirty very quickly and can be just as much a problem.

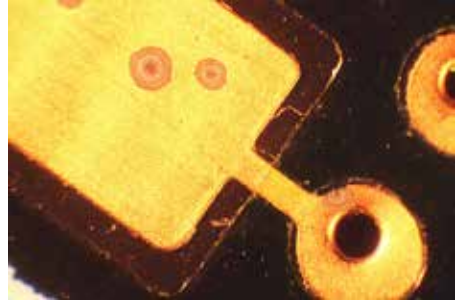
Gold Tab Contamination



It is common practice to mask gold edge contacts during the printed board assembly and soldering processes to avoid unnecessary contamination. It is very difficult to clean surface residues from gold contacts without damage. It's even more difficult to remove solder spots from any gold surface after soldering. The image shown below has edge contacts that

are contaminated with resin from very inexpensive masking tape. If the board is subjected to heat when passed through a soldering process the resin will remain on the surface of the gold on the bare laminate which is very difficult to clean. It's much better to use Kapton® tape, its more expensive but provides much better process protection.

Solder Spots



So what are solder spots? They are often a problem in modern reflow assembly, in fact in any process that involves solder paste. The spots are visible on the surface of pads which have not been pasted prior to reflow. The spots are seen more commonly on copper, gold or any surface which is not fusible during reflow. The spots can be tin/lead or lead-free alloy which become visible due mainly to the different color of the pad surface and the wetting action which takes place during reflow. If the spots were on a solder or silver surface there would not be much of a problem, out of sight out of mind. Some companies do apply rigid standards or apply the IPC guidelines very vigorously, failing the products at final test or during goods receipt if products are contracted out.

The images at the top of the page are typical of solder spotting on gold pads

Solder spots can be seen during a reflow simulation test using glass hour glasses placed over paste deposits on boards or test coupons then subjected to the reflow process. These samples allow any paste spitting to be visible after reflow on the surface of

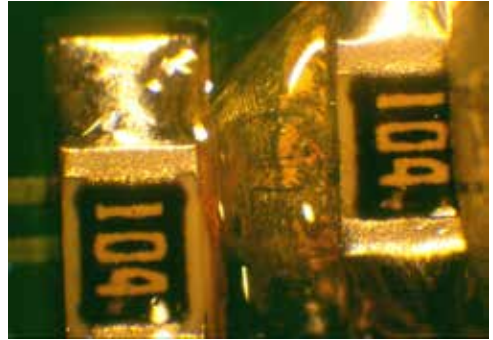
the glass. This test samples can also collect the volatile material from the surface of the board and paste deposit for analysis.

The four images below show the surface of the glass with the paste below in different stages of the reflow process. The final image shows the surface of the glass with the volatile material on the inside surface of the hour glass.

If the surface of the pads are to be used for interconnection then any contamination may not be acceptable. Contact strips, LCD interconnection or key pads are examples where solder contamination of course, mechanical connection failure or intermittence. This would, have cause be related to the position and the size of the spots. It is, however much easier to just reject the products than make a judgment call but that is a costly option. Depending on the cost of the product, make repair viable the spots can be removed without any obvious signs.



Conformal Coating Failure



Coating lifting due to the chemical reaction on the board surface

If contamination on a printed board assembly prior to coating is soluble, it can repetitively dissolve and crystallize after coating (between the coating and the substrate) as moist air penetrates and then dries out over time at the interfaces. The contaminant may be ionic and will induce an osmotic 'pumping action' pressure, which can compromise the protective abilities of the coating, promote poor coating adhesion and/or dewetting, and in the most extreme cases cause voids and bubbles that permeate the surface of the coating. This condition is known as *vessication* or *measling*. This not mean the no clean is not suitable for use with coating, it's just engineers need to control their process and be fully aware of the correct material selection procedures and work closely with both suppliers.

This degradation can be made worse if moisture penetration reacts in unpredictable ways with assembly materials and residues left on the board after production (including oily organic particulates left by any form of manual handling). Ionic contaminants on insulation surfaces are particularly damaging, since they can compromise electrical contact of in-circuit test probes, cause electrical leakage and corrosive degradation of the circuit elements, and ultimately lead to failure of the assembly.

Ionic contamination will also cause 'measling' of conformal coatings that is not only cosmetically unattractive, but will also result in rejection of the completed assembly under most supply contracts. Prime sources of ionic contaminants include rosin flux residues, acidic soils in the form of perspiration and fingerprint residues from manual handling and previous chemical processing steps such as etching or plating. Whilst rosin itself is non-ionic, it too should be removed since it partially encapsulates ionic residues from flux activators. Ionic contamination can be measured using a range of test methods. These can determine the amount of ionic contamination remaining on an assembly after various manufacturing procedures.

Although there are many application where a combination of no-clean and conformal coatings are used strict controls must be in place to monitor the remaining residues after wave, reflow or selective soldering. If the flux residues are proven via testing to be inert the quantity of remaining residues may be an issue. They may not directly lead to corrosion and failure but during temperature or product cycling the material will expand and contract leading to coating lift and a further opportunity for moisture to mass in selected areas of the circuitry.

The Cleaning Debate

Four distinguished experts in the cleaning industry and one distinguished publisher met at a recent industry event to discuss challenges in cleaning. The panel included Inventec's Jan-Henryk Serzisko, Zestron's Ralph Hoeckle, Factronix' Thomas Otto, who represents PBT's cleaning equipment, and Riebesam's Nikolaus Stiehl. The discussion was moderated by Global SMT & Packaging magazine's publisher and editor-in-chief, Trevor Galbraith.

Topics Covered

- Cleaning under low standoffs
- Cleaning chemistries & nano-coated stencils
- Choosing inline vs. batch cleaning systems
- Cleaning requirements for conformal coating
- Cleanliness testing

If a customer's considering implementing a cleaning program, what's the best approach?

Jan-Henryk Serzisko: As an employee of a chemistry company, I would of course say talk first to the chemistry provider. It's important to involve as soon as possible the equipment manufacturer, but I think the first approach should be to talk to chemists and then choose the equipment.

Ralph Hoeckle: At the end of the day what the customer wants is a stable-running process that gives him the results he needs. Defining the process is quite time-consuming because you have a wide selection of cleaning machines and a wide selection of chemicals. Ideally you go somewhere where you can test chemicals and machines under different conditions together with your parts and get a quick indication of what is a good way to go, and then take it from there. So process is, for me, the key word.



Thomas Otto: I absolutely agree with that. The best experiences we've had is always when the customer first does some testing with chemical solutions and defines the best mechanical process, whether it is ultrasonic, if he's allowed to do ultrasonic, spray. Depending on that process, and depending on the number of boards, the size boards, or the kind of object he has to clean, the throughput that is required, then he can decide on a specific machine that matches his requirements.

Nicholas Stiehl: This is also how we always proceed.

A lot of companies today are doing high-mix manufacturing, so it's not one size fits all. They're going to have different sizes of board, different types of projects they're going to have to clean, but certainly starting with chemistry may be the best way.

One of the biggest challenges we have in cleaning is of course cleaning under low standoff. Are there any components that you cannot clean under, where they're so low to the board that it's just impossible?

RH: Actually, we haven't seen that so far, and we do a lot of business with Asia, where more or less the really high end and lowest of components in the mobile phone industry are defined. The whole landscape of mobile phones is smaller and smaller and lower and lower. We haven't seen anything we can't clean under so far, but it's possible that it may come in the future.

The market reflects that 95% of all cleaning processes are water-based, so water plus some chemistry to clean, with water rinsing—works very well. But there are very specific cases where a solvent-based process might be suitable. And we offer that as well, but it's really, if the technical requirement is there, then it's possible to do it, but again, water-based processes have advantages.

So far the lowest standoff we've seen is 20 μm . That's on volume production, not on what I would call prototyping. And so far we can clean it without any problem—but you need the right machine, the right mechanics to be able to do it.

NS: Our experience as an equipment manufacturer is a little bit different. It is true that majority of the cleaning processes are water-based so far, but the demand for better results and improved and different technology has increased dramatically in the last two years. As the short distance between the board's tracks and gaps has decreased, it is becoming more apparent that you need a different chemistry solution.



Nikolaus Stiehl, Riebesam

JHS: I agree with Mr. Hoeckle that most of these low standoff components are being produced in China, in mobile phones, but you must not forget that these low standoff components are also used here in low-reliability environments. Your mobile phone has a lifetime of probably one to two years, and then your contract gets renewed and you get a new mobile phone. He's right. You can clean with water under these components to achieve this level of reliability.

But if you go to really high-reliability applications, then you need, most probably, another process for cleaning. Yes, we can cover maybe 80-90 percent of the cleaning requirements with water, but as Mr. Stiehl said, "We are at the turning point." Our feeling is that solvents is the future in high

reliability applications.

For non-vital reliability, yes, you can use water, but as soon as you get into real high reliability, we would recommend solvent-based.

What sort of effect does the impingement factor have on cleaning underneath low standoffs and the types of nozzles you use?

TO: PBT invested a lot of time and money in developing tools to show the results of different nozzle types and different spray angles, to find out the best solution to get underneath these low standoff components.

The best solution that PBT found is definitely a 90° angle to the board from both sides to achieve the best force to get underneath the components.

Recently, nano-coated stencils have been introduced. There are a couple of companies doing it: LaserJob, which I think were the pioneers of that technology, and DEK have also got their nano-coating material. Does this bring any challenges in terms of the chemistries used for cleaning stencil treated with these nano-coatings? Presumably, when you clean the stencils, you don't want to remove the nano-coating as well.

JHS: Up to now, we haven't seen any negative impact, so we don't have a special



Thomas Otto, Factronix/PBT

cleaner for it. We will make a long-term analysis for this, but at the moment not. If you have chemical nano-coating probably it might run a higher risk, but with physical nano-coating, we don't see any problem.

RH: That's the first question a customer asks: Can I continue with my current cleaning process? We've done testing with all the key suppliers, we've tested all their technologies of nano-coating with all our cleaning agents on multiple cycles—basically the lifetime of a stencil. Under normal circumstances, using the range of products we have, we have seen no issues.

At what point should a customer decide whether to use an inline process or to use a batch cleaner? What's the crossover point? If he's doing more than 100 boards a week, for example, should he go inline?

NS: It's a matter of the output that the machine has to be able to do, is it a one-shift process or daily process, and this based together with the process as it is defined with the chemistry supplier, and the analysis that has been done. Either you could end up with a batch machine or an inline machine for more than 100 boards. Both are possible.

Does the mix of manufacturing have any impact on the decision?

TO: Sure, but there are so many factors to decide with that. There are so many different types of inline and even batch systems. You can have kind of a belt system, you can have kind of an inline system working with different baths where you just move the basket from one tank to the other bath. The drag over—the consumption of cleaning agent as the board is moved to the rinse chamber—is also an issue that you have to put into your calculation to decide which system is right for your needs.

RH: To the core of your question—inline or batch—in my point of view, as far as we see

it, there is also the matter of required automation. An inline machine has a very big footprint, and you have it in one spot. If you want to decentralize your cleaning, if you have different boards in different locations and you want to run different processes, then maybe, even for a total high throughput, it might be better to have decentralized batch machines—no matter what kind of batch machines.

TO: It could be different ones.

RH: Exactly. Depending on the requirement of that specific substrate for a contract manufacturer, for example. But if you have one substrate or a limited number of substrates, if you can run one process defined at your very highest throughput, then for sure an inline machine is better.

Most of these batch machines they're an offline thing and there's usually one or two of them in the factory in a room somewhere, they're not usually on the factory floor or in the line.

RH: Throughput is really the key word. If you have low throughput, you don't buy a very big machine. You buy what you need, which is a small machine you can put where you have the space. You know it's one maybe square meter or two square meters, versus an inline machine. Also a batch cleaner of course is smaller equipment, it's less costly, and the cost of ownership is also lower. No matter if it's solvent batch cleaner or water-based batch cleaner. But it really depends on throughput first of all.

How important is it for some of these companies to have closed-loop systems?

TO: Especially if you're talking about wastewater, it's the one and only issue. You need a closed-loop system to filter as much as possible before you get the water or cleaner going to the drain.

Some manufacturers are conformal coating without cleaning, and when I say 'some,' it's probably in many cases most, but really, are there a lot of inherent dangers in doing that? Surely they're trapping an awful lot of soil underneath the coating, leading to electromigration problems and things like that. Are they not storing up problems for future?

JHS: For us it's a clear recommendation to clean before coating because you're creating a greenhouse effect under the coating with residues left on the boards. You must not forget humidity is coming out of the boards, so you get electromigration problems, which were not so much a problem in the past when you had really huge distances between the tracks, but tracks are getting smaller, and so electromigration is becoming an urgent issue. We definitely recommend cleaning before coating. For adhesion, cohesion issues—



Jan-Henryk Serzisko, Inventec

That's a good point. You get better surface tension for adhesion.

JHS: But also for reliability. In the long-term, mid-term, you get issues with reliability if you do not clean before coating.

RH: Every coating supplier, and we talk to all of them, knows and recommends that if you want to have the best possible adhesion, clean. And all of us would be happy if they would do more cleaning, because that's what



Ralph Hoeckle, Zestron

we do, but at the end of the day the customer wants to avoid the cost. So the deciding factor is reliability testing. They will do the coating without cleaning. If it passes a reliability test, they will not clean. If they

don't pass, they think about cleaning.

We have seen some customers who ask should I do no-clean and coat or should I clean and not coat? Which is interesting. We have seen cases where customers have fewer issues with electrochemical migration or other problems when they clean and not coat. It's because they just removed the critical substances that are on the surface that cause the problem. If you coat on dirt, electrochemical migration actually happens underneath the conformal coating. Some people think that the mechanical barrier can avoid the migration. It doesn't. It's like a mushroom growing through concrete. So we all would love if people clean more, of course, before coating, and I think it's moving in that direction actually, because reliability requirements are increasing.

When it comes to testing for an acceptable level of cleanliness, what do you think is an acceptable level using ROSE testers, which are the common method of test?

NS: It's a very good instrument for testing but it should not be the only one. You have to do also other analyses to come at the end to the result per case, because each case is

also different. It's not always the same. But ROSE test is a must in-between.

TO: Exactly what Mr. Stiehl said. You need a selection of different tests, and after a while you will be very experienced about where the critical parts of your PCBs are: underneath components or in small gaps, where you should look first. A microscope, of course, is the first and probably the most helpful tool in the first step to find out about the contamination.

But of course you can see so much underneath the components but you want to avoid doing destructive testing and try to leave the board intact.

TO: Sure, you need other kinds of tests of course.

Jan, do you have a view on the testing systems and the acceptable level of cleanliness?

JHS: The acceptance level is defined in the standards, and I think to reach this is not a problem for either the equipment or the chemistry that we are offering. What's more indicative is the requirement of the customer. What does he want to achieve? What does he want to do afterwards? We don't want to overdo the cleaning if it's just cosmetic. You don't have to spend so much money. But if you are going to bump afterwards, to coat afterwards, if you have a lifetime reliability of maybe ten or twenty years, then the requirement is far tougher than the standards. So when the customer defines what he wants to achieve, then we see how we achieve it.

NS: But sometimes the customers does not know it.

TO: That's why we are specialists.

JHS: Yes, but, we need to talk. It's a communication with customers, with equipment manufacturers, and it's a partnership at the end of the day that we want to achieve.

Ralph, obviously most customers are not going to be ROSE testing all the time on a continuous basis, but would you assume they would test at the beginning, when they're trying to do the prototyping and setting up the process—?

RH: Both. Nowadays even with a no-clean process you can be way below the standard for ROSE testing. If you clean properly, no matter which kind of process, you can go to 0.1 micrograms. So ROSE testing is not “Is my board clean?” It is mostly used to monitor the process. If I get a pattern of stable results from my cleaning process, I can guess that the result will be the same at proper conditions. So ROSE testing does not define the real cleanliness. It does not define the cleanliness of the substrate. It gives you an indication of where you are in your process. It's a very cheap method and it's an indus-

try standard, so that's why people still do it. There is SIR testing and other methods which are just more costly and more complicated.

So does the panel agree that ROSE testing is probably the most common and easiest-to-use testing methodology?

RH: I would say it still is, because there is nothing else, nothing which gives you a figure out of a machine, which is what engineers want.

I want to thank our panelists for taking the time to get together for this informative and useful discussion. The full debate is also available on video—access it free at tv.globalsmt.net. —Trevor Galbraith

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They made this cleaning guide possible. We hope you will find it beneficial.

NPL Online Defect Database

National Physical Laboratory (NPL) have created an interactive defect database allowing engineers to search through a range of defects covering components, printed circuit boards coating, cleaning and assembly problems. The aim is to add more process, material and environmental defects with the support of engineers by online submissions from readers.

Any database will take time to populate with industry defects, but with worldwide industry cooperation and introducing defect types from research studies across the world this will result in a unique resource. A very practical benefit is its online global availability 24/7 to shop floor operators as a reference and training resource. The NPL database also provides access to over 150 technical research reports from the NPL Electronic Interconnection Team covering typical process and reliability issues faced by industry <http://defectsdatabase.npl.co.uk>

NPL
National Physical Laboratory

The UK's National Measurement Laboratory

National Physical Laboratory Industry Defects Database

Name (*)
Company (*)
E-mail (*)
Failure title
Upload Image
Failure Category -Select a failure category-
Description:
Probable cause:
Solder alloy: -Select a solder alloy-
Soldering Process: -Select a soldering process-
Failure location: -Select Failure Location-
Number of failures found:
Volume of this product: -Select Product Volume-
Product Application: -Select Product Application-
Specify if others:

(*) These will be kept confidential and will not be included in the database.

The front page screen shot of the NPL Defect Database shows where engineers can query the database for cleaning defects, process, alloy type etc. Alternatively if the defect is not available then it's easy to submit a photograph for inclusion and discussion in the online database

NPL have been actively supported by IPC who feature its “Defect of the Month Video”. The videos have highlighted a common process problem or defect and provided some simple solutions. In most cases including photographic examples or videos show

defects happen to make the failure modes more understandable. “Defect of the Month” video can be viewed on line via the IPC home page: www.ipc.org

The below screens show an example of one of the defects found after a search of the database providing information on the defect, how it occurred and possible corrective action. Selecting the image provides a larger view of the defect and the opportunity to print out the results for shop floor staff and discussion.

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Search
Enter search term here

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Metadata

Showing Defects Database

Title:	PCB solder joints
Description:	These two pins have soldered on the first face of the pins which should normally be easily seen during inspection as the magnification of the pins have not formed under the body of the part.
Rootable Cause:	This is probably due to solderability problems with the printed board and are not related to the lead free process.
Number of Defects:	1
Failure Alloy System:	Lead-free
Defect Category:	Assembly/finishing
Defect Location:	Printed
Defect Volume:	Medium (10 to 50 per week)
Defect Application:	Substrate applications
PLC component terminals:	
Underlying processes:	Review the solderability of the printed circuit inserts prior to assembly or consider how the solderability has been degraded during the assembly process
Possible Solutions:	See Good Practice Guide No. 64 on Solderability Testing protocol to NPL. For details contact Ling Zou (email ling.zou@npl.co.uk) Telephone 0209 543 4005
Further Details:	

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Showing Defects Database



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The NPL Industry Defects Database is available 24/7 to allow readers to search for solutions to common problems or submit defects online with full details or requesting advice and a possible solution to the process issues or failures at <http://defectsdatabase.npl.co.uk>

NPL Cleaning Related Reports & Good Practice Guides

Here is a list of the cleaning related reports available free of charge to engineers to download to assist them with their cleaning process development. The project reports can be downloaded direct from the database.

- An Assessment of the Suitability of Current PCB Laminates to Withstand Lead-free Reflow Profiles
- Development of a New Surface Insulation Resistance (SIR) Test Method
- Development of Surface Insulation Resistance Measurements for Electronic Assemblies
- Procedure for Process Validation With Surface Insulation Resistance
- Effect of Voltage, Pattern & Board Finish on SIR Measurements for Fluxes
- The Role of Permeability and Ion Transport in Conformal Coating Protection
- Evaluation of the Ability of Conformal Coatings to Inhibit Tin Whiskering
- Measuring Anionic Contamination of PCBs & Assemblies using Ion Chromatography
- Preliminary Measurements of Solder Flux Residues in an AC Environment
- Protection Performance of Conformal Coatings in Harsh Environments
- Susceptibility of Lead-Free Systems to Electrochemical Migration
- Testing Conformal Coating Protection for Electronic Assembly in Harsh Environments
- Measurement of the Propensity for Coatings to Inhibit Tin Whiskering

IPC Cleaning Standards and User Guides

The following are a list of IPC documents on cleaning processes and assessment of the cleaning process performance and can be purchased direct from the IPC via their website www.ipc.org or via any of their worldwide distributors.

- IPC CH-65B Guidelines for Cleaning of Printed Boards and Assemblies
- IPC 5704 Cleanliness Requirements for Unpopulated Printed Boards
- IPC 7526D Stencil and Misprinted Board Cleaning Handbook
- IPC 9201A Surface Insulation Resistance Handbook
- IPC-5701 Users Guide for Cleanliness of Unpopulated Printed Boards
- IPC-5703 Cleanliness Guidelines for Printed Board Fabricators
- IPC 5702 Guidelines for OEMs in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards

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