Guide to PCB Surface Finish Defects

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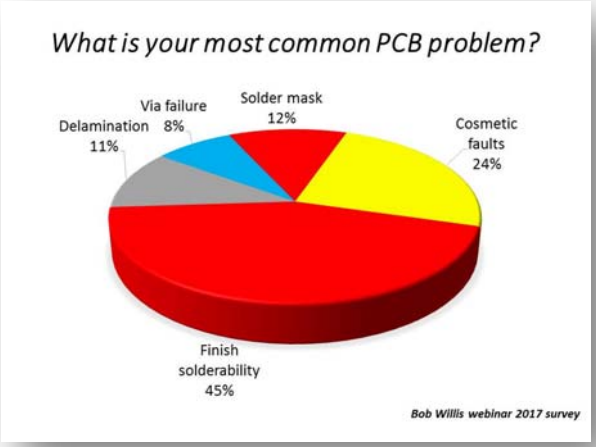
Introduction

Welcome to this SMART Group Defect Guide

Our latest SMART Group Defect Guide, is aimed at final PCB surface finish. These finishes are provided to protect exposed copper and to maintain solderability of the pads and through hole termination points to allow successful soldering in reflow, wave, selective and manual processes

The choice of solderable coatings in the industry has grown over the years with multiple vendors offering alternatives for all main coating types. Originally, we used fused tin/lead, solder level, copper OSP or flux lacquer coating. With the move to smaller pitch and the introduction of lead-free we have many choices which can make selection difficult and an issue for the supply chain to provide the options a customer demands. Most suppliers focus on just two or three coatings so have options but can control their process. Our latest survey of 100 engineers shows that surface finish is still a common cause of process issues for users assembling bare PCBs



With information to help the newcomer and expert user we hope you find this a useful guide and ask you to pass on some SMART Group knowledge to your team, your customers and suppliers. If you have any other defect types relating to surface finishes why not add them to the NPL Defect Database http://defectsdatabase.npl.co.uk or send them to technical@smartgroup.org

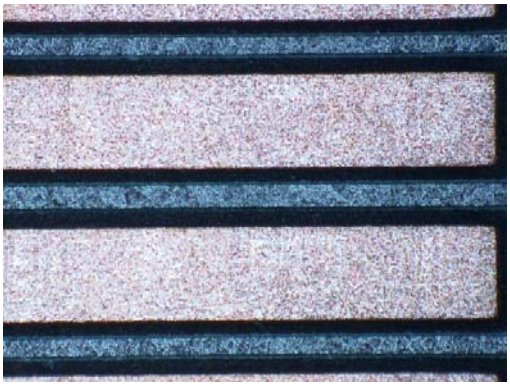
Many thanks again for support to SMART Group

Bob Willis
SMART Group Technical Committee

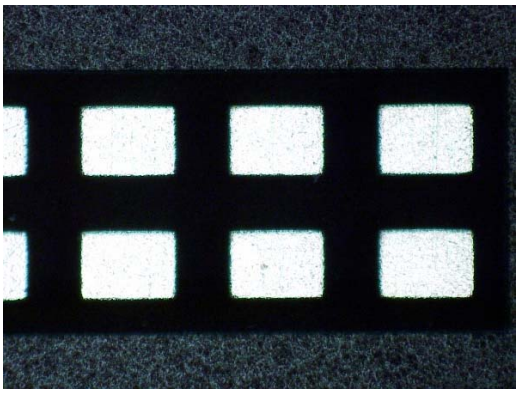
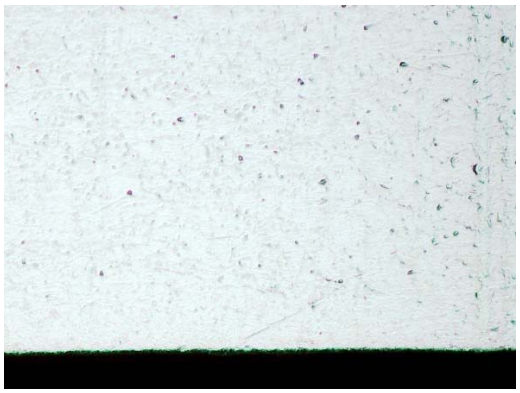
PCB Surface Finish Reference Images

The following example images are typical of printed circuit boards with different surface finishes. A surface finish is the final coating on surface mount pads and through holes when supplied by the manufacturer. The surface finish is specified by the assembler based on the process for assembly and environment the final product may be exposed to. Using the correct surface finish is very important to obtain good yields during assembly and soldering, the introduction of fine pitch & lead-free assembly increased the options

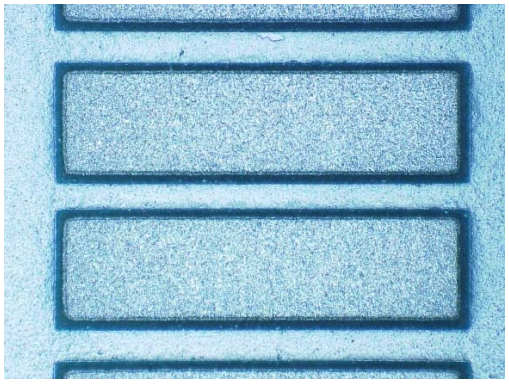
Copper Organic Solderable Protector (OSP) (50 – 200x)



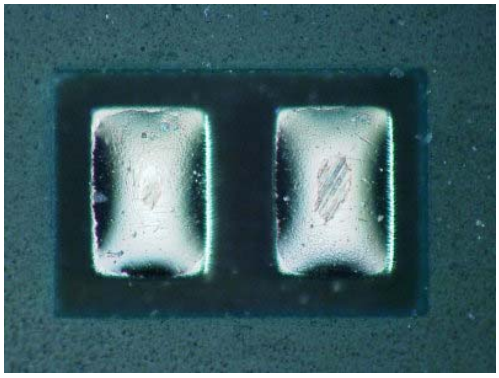
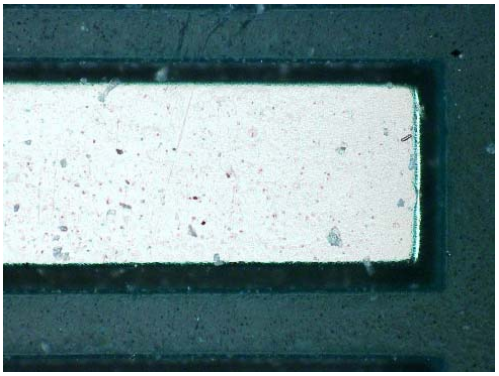

Immersion Silver (50 – 200x)

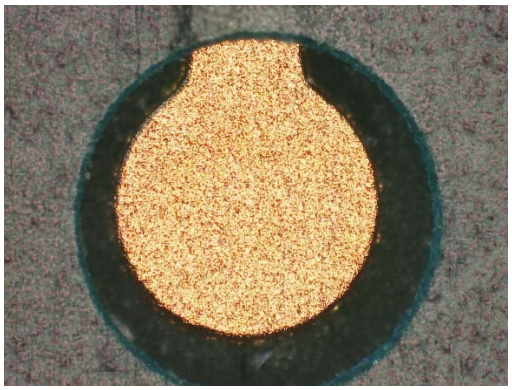
Immersion Tin (50 – 200x)




Solder Levelled Lead-Free (50 – 100x)

Nickel Gold (50 – 200x)




Whichever surface finish is specified by the designer or assembly engineer it is very important that they understand the material, its application in PCB manufacture and how to assess the quality of the coating. They should also know the specific type and supplier of the finish chemistry used and the method used by the manufacture to test the solderability of the boards prior to despatch. This is important to avoid the debate about what is or is not acceptable. Solder float and dip testing is not reflective of modern reflow technology

Engineers should be fully aware of the packaging of the boards and the length of the supply chain prior to assembly so they can correctly judge changes in solderability that may occur prior to the first assembly steps. Often prototypes and NPI boards are produced from boards made yesterday and delivered by aeroplane. Volume manufacture is often based on batches of boards that are much older and have spent the first part of the life on a ship. It is recommended that goods receipt and technicians on the assembly line know how to recognise different surface finishes and if they are acceptable when first unpackaged for use. They should have some reference like the images in this guide but, better still, examples from their own supplier

It is recommended that the quality department take low and high magnification images of known good surface finishes from the supplier that can be used as a reference by staff. The images should accurately show the colour, the surface texture and evenness of the coating. In the case of thin coating the surface of the copper topography. There should be no evidence of solder mask residues on the surface of the pads causing lack of proper surface coating of the pads or through holes. The images provided here are satisfactory, but may not represent the colour or surface preparation of your supplier

Printed Circuit Board Surface Finish Introduction

The following is a brief description of the most common coatings used in the industry and generally referred to as surface finishes or solderable coating.

Immersion Tin

Immersion processes like silver and tin have an organic deposit as part of the process that reduces the oxidation that would be expected with a pure tin or silver surface. Tin and silver dissolve into the solder and become part of the solder joint and with such a thin coating it's relatively undetectable. Both tin and silver are dissolved during soldering so the solder joint forms directly with the copper surface just like copper OSP. On gold boards the solder forms a joint with the nickel after dissolving the gold.

Just like silver tin is mainly defined by the control of the printed board process although the assembly operation can have a major impact on the solderability. The key to the process is eliminating the copper/tin intermetallic forming at the surface of the coating. Now with 1um coating and a less porous finish this provides a more stable coating for assembly. It is being used for boards that also incorporate press fit connectors as this does benefit the insertion forces with a degree of lubricity. Having extended factory hold times before second side reflow or selective soldering will affect wetting just like delay in second stage assembly operations

See IPC-4554 Specification for Immersion Tin Plating for Printed Circuit Boards

Immersion Silver

The coating is an immersion silver coating of between 0.08-0.1um which also incorporates an organic layer as part of the process. The silver "Alpha Level" coating is maintained in a highly solderable state by the organic coating. Although Cookson were the first to offer this coating there are other suppliers also providing silver solutions like MacDermid.

The surface coating has all the benefits of any alternative finish and resembles the tin coating when soldered. If during soldering the solder dose not fully wet the pad surface it is not as obvious as with copper and gold pads. In the case of unsoldered holes or test pads there is no visible gold or copper, which to some engineers is an emotive subject. The coating cost in medium to high volume is equal to or less than nickel/gold.

Like any alternative coating, provided it is processed correctly by the circuit board manufacturer, the surface will remain solderable even after multiple heating cycles. Hence it is compatible with double sided reflow. Issues have been seen with washed off boards and the use of temp solder mask coatings. The basic coating process must be reviewed with the supplier to make sure he is using guidelines from the chemical supplier. A key issue is the control of the process and the final rinse and drying stages.

See IPC-4553 Specification for Immersion Silver Plating for Printed Boards

Copper OSP

The protective coatings are generally defined as organic coatings referred to as OSP, (Organic Solderable Protector or Organic Solderability Preservative). The most common coatings are benzotriazole and imidazole; both are organic nitrogen compounds. Benzotriazole has long been recognised as an anti-tarnish coating used in the general metal finishing industry. Inhibitor coatings are extremely thin and essentially invisible on the copper surface.

The coatings protect the copper by chemically bonding to the surface and prevent the reaction between the copper and oxygen. The coating may be applied by dip or spray coating and followed by a rinse operation to remove any residues remaining on the solder mask surface. If required, the coating may be removed and re-applied to rejuvenate a surface which has become un-solderable. If required, the surfaces would need to be re-cleaned with an acid etch and rinse prior to re-treatment.

See IPC-4555 Specification for Organic Solderability Preservative (OSP) for Printed Circuit Boards (Committee Draft Never Released)

Nickel Gold

Gold over nickel has become very popular finish for surface mount boards particularly for fine pitch and mobile communication products like mobile phones. They have provided an ideal assembly surface, highly solderable and an aid to inspection due to the contrasting colour between component leads, solder and the solder paste. When wire bonding is required for chip on board applications gold over nickel has been the finish of choice when bonding and soldering is required. The cost is generally the same as solder levelled boards in medium to high volume.

Exposed outer copper surfaces are coated with solderable finish of electroless nickel, 3 microns minimum to 7 microns maximum with finish of immersion electroless gold to a thickness of 0.03 microns minimum to 0.07 microns maximum and maintain the solderability for a minimum of 12 months.

IPC-4552 Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

A second choice in terms of gold over nickel is electroless nickel/electroless palladium/Immersion gold (ENEPIG). The palladium is provided as a barrier to stop the diffusion of the nickel to the surface of the thin gold. It may also assist with the reoccurring problem of black pad where the gold attacks the exposed nickel layer at the nickel grain boundaries during plating. This problem can lead to weak joint on boards and is predominantly due to poor process control in manufacture of the PCB

IPC-4556 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) Plating for Printed Circuit Boards

Solder Levelled

The solder levelling process became popular in the early 80's and is still a commonly specified finish. Originally, eliminating the solder coating under the resist reduced the possibility of the resist lifting during the assembly soldering operation. It provided a guaranteed solderable surface from the PCB manufacturer. It also provides a further benefit to the assembler of stressing the board. If the solder resist coating was poor or the lamination of a multilayer circuit was questionable then it would generally show up during exposure to the molten solder bath prior to shipment to the customer. Originally the coating was more expensive than traditional tin/lead plated finish but this is not now true.

Solder levelling requires a process panel to be dipped into a solder bath of either tin/lead or lead-free alloy after first passing through a light etch then fluxing. The process is mainly conducted vertically however horizontal systems are also used. As the boards come out of the solder heated air knifes blow off excess solder typically leaving thickness ranging between 2-15um

Tin/Lead Reflow

Tin/lead was the standard finish in the industry for many years due to its use as an etch resist to produce plated through hole boards when subtractive processes have been adopted. It originally provided an ideal production solution to protecting the copper surfaces during the final copper etching process. It has also proved useful as it provides a solderable finish for the protection of the copper pads and tracking for subsequent soldering operations. The thickness was between 5-10um. Now tin is commonly used as the etch resist in manufacture.

The tin/lead plated finish was reflowed as part of the PCB process to overcome slivers and to provide an alloy of tin/lead rather than a plated surface. The long term solderability of the reflowed surface was superior

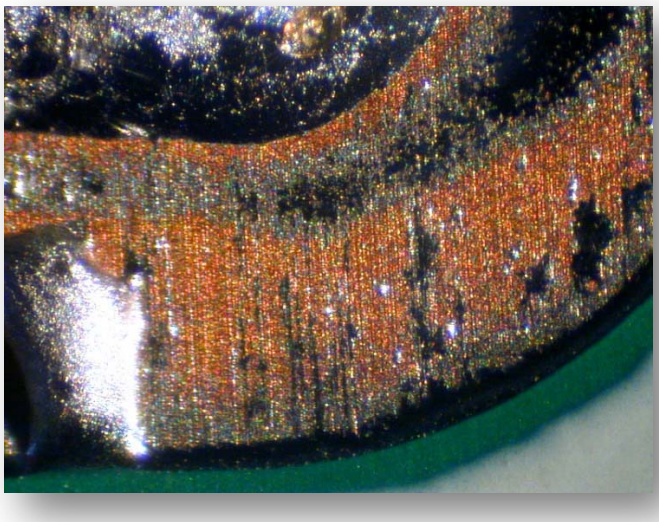
Plasma Coating

A new surface coating process to the industry from Semblant. The coating is produced in a plasma chamber and coated when the boards are in their process panel, although finished boards could be treated. The chamber allows a set number of panels to be produced at one time depending on the size of the system. The use of plasma chambers is not new to many high-end PCB fabricators as the process has been used for de-smearing resin on through hole connections prior to plating. The actual coating thickness is extremely thin based on the process cycle of the chamber and its performance. The coating completely covers the panels and is in the nano metre range on the copper surface so it looks like copper OSP.

The coating is hydrophobic so tends to repel moisture and other liquids so it is also offered as a possible conformal coating. It does have good performance for multiple reflow soldering process due to the high temperature capability of the coating. During reflow most of the flux residues seem to remain at the joint interfaces where the residues do not wet out from the pad or joint surface. The surface can be conformal coated after a pre-treatment stage. The author has not yet had the opportunity to run trials on the finish with other processes like wave, selective and intrusive reflow.

Printed Circuit Board Surface Finish Defects

Poor Solder Wetting

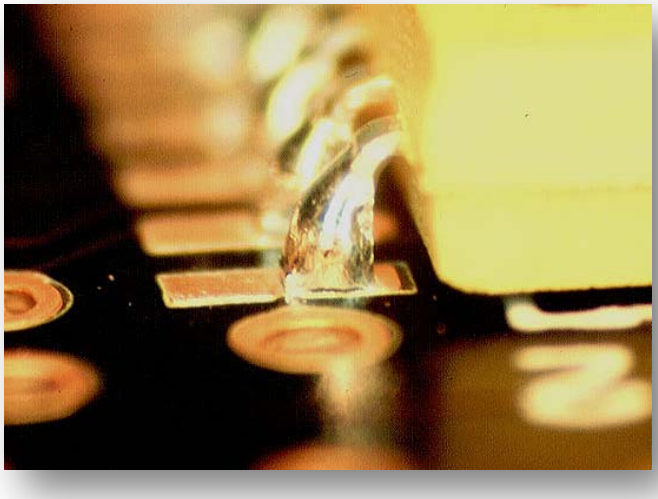


Poor wetting is visible on a copper Organic Solderable Protector (OSP) pad after selective soldering. The lead-free solder has failed to wet the surface of the copper pad but does show wetting to the barrel. In this case the copper shows it has been exposed to a brushing step in PCB manufacture indicated by the parallel lines on the copper surface. It is poor practice to have a mechanical cleaning step on copper prior to OSP application. Some companies have used mechanical cleaning to rework products or increase solder mask adhesion. However, this will always impact the solderability

Copper Pad Dissolution

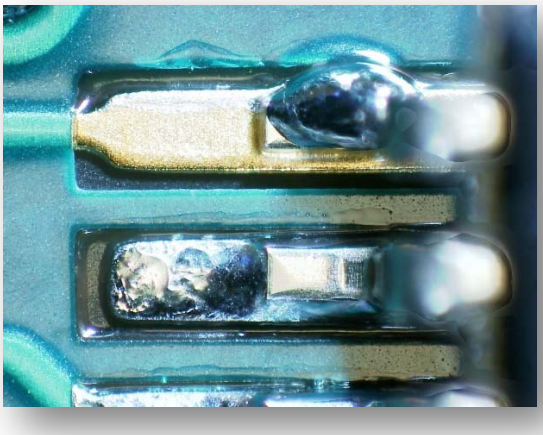
The through hole pad surface looks to have de-wetted after selective soldering with tin/silver/copper lead-free alloy. The copper pad on this board has been virtually dissolved by the solder due to a combination of the alloy used, the temperature, soldering time and solder flow rate. All surface finishes, except for nickel gold, are susceptible to copper erosion if the assembly process is not controlled. The first examples of copper dissolution were seen during through hole rework using solder fountains and during the early days of lead-free solder levelling where double dipping or long immersion times were used to overcome thermal demand of the design

Solder Wicking During Reflow



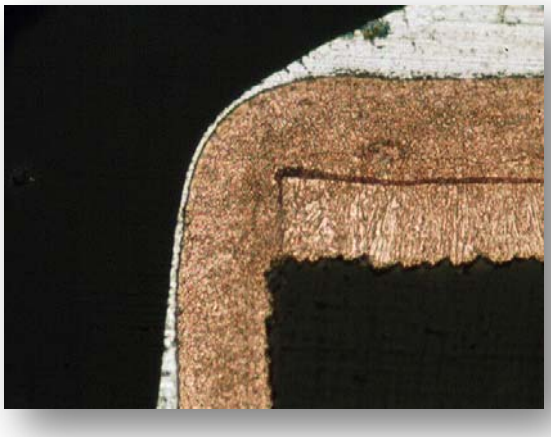
Solder wicking has taken place on this Small Outline Integrated Circuit (SOIC) gull wing package, the solder paste has reflowed successfully and wetted to the lead and not the pad due to its poor solderability. In this case the cause of poor wetting was a poorly defined cleaning step prior to printing and reflow in the assembly process not the original copper OSP coating supplied on the circuit board. Process engineers need to evaluate any process step that may impact the soldering operations during assembly. Its important to remember there are often two, three or four soldering steps during some processes. Cleaning should, where possible, be the final process or consider a surface finish which is more compatible

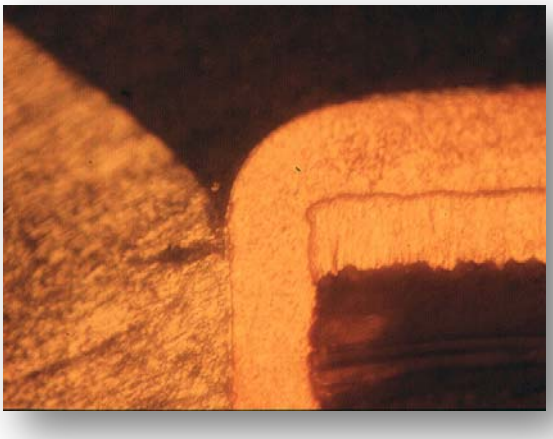
Solder Wicking During Reflow



Solder wicking has occurred on the resistor network terminations. The solder when reflowed has wetted to the termination and not the pads on the gold board. This will be due to contamination on the surface of the gold that the flux could not remove during reflow. In this case it was due to cleaning the boards after poor printing, basically a paste wash off in a poorly defined process. Its perfectly possible to wash a board after poor printing and reprint but some surface coatings may not be compatible or the process needs to be evaluated and controlled. The image on the right shows the same type of wicking defect on a gull wing lead with the solder reflowing preferentially to the lead rather than equally between the pad and lead

Weak Knee





The weak knee effect is a term originally coined in the USA for solder levelled boards. During wave or selective soldering when the solder fails to wet or pass over the edge/knee of a plated through hole there is poor wetting on the sharp edge of the hole. During solder levelling and during tin/lead plate and reflow it is possible to have less that 1um of coating at the knee of the hole as illustrated in the example. We have not seen the same issue with solder levelled lead-free alloys, this may be due to the high level of tin. The solder coating can be so thin at the edge of the hole that most of the tin is consumed over time forming a lead rich surface. This is much less solderable that the tin/lead and hence it appears as a process problem during through hole soldering.

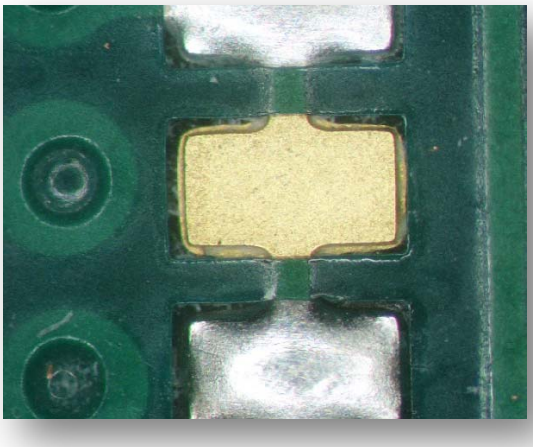
Solder Balls on Pads

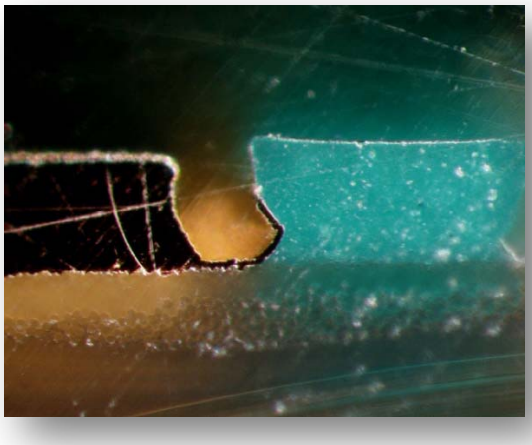
Solder balls on the surface of pads is due to contamination on the surface of the gold pads prior to paste printing. The solder paste has reflowed and as there were no terminations to pull the solder away from the poorly wettable pad, the solder has formed a ball. In this case the root cause of the problem was a poorly defined board cleaning step prior to paste printing. This type of defect can occur on different surface finishes but less likely on a solder levelled coating. Using a simple dot pattern solderability test strip on the waste areas of the board or panel allows assessment of any board without waste, for details on the test method contact technical@smartgroup.org

De-wetting on Pads

De-wetting of tin/lead solder on the surface of through hole pad may have been due to the copper pad preparation or the thickness of the solder coating in the original PCB manufacturing process. De-wetting is a less common defect today but is often misquoted in manufacture

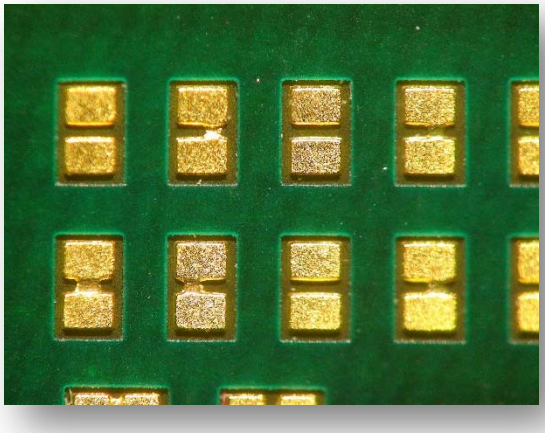
Nickel/Gold Foot

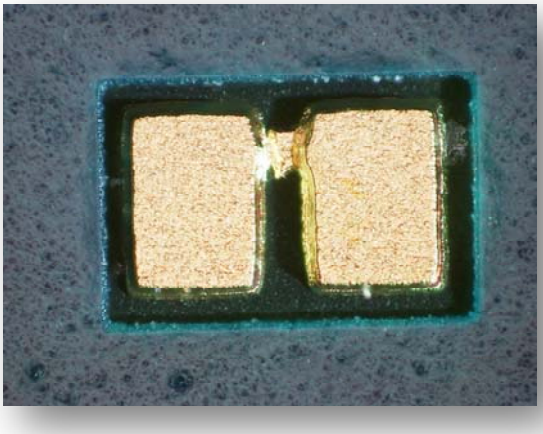




Nickel/gold foot is an unusual formation that can lead to shorts and reduction in surface insulation. The photograph shows a gold halo around the surface mount pads. Nickel has plated onto the surface of the laminate and the edge of the solder mask. This has also allowed gold to coat the surface of the nickel reducing the minimum design gap. Microsectioning of the nickel/gold foot clearly shows the plating defect. The nickel can be seen to extend from the bottom of the pad across the laminate and up the solder mask wall. This seems to be a more common process defect on PCBs and one that more users should discuss with their suppliers as an issue of quality control in board fabrication

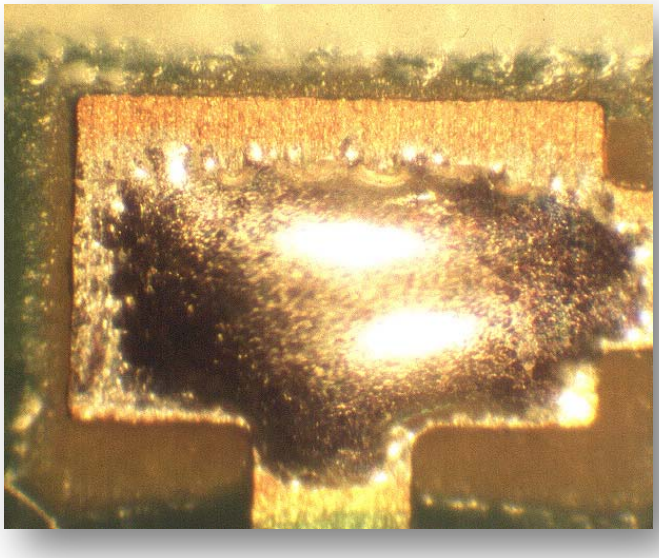
Short Circuits





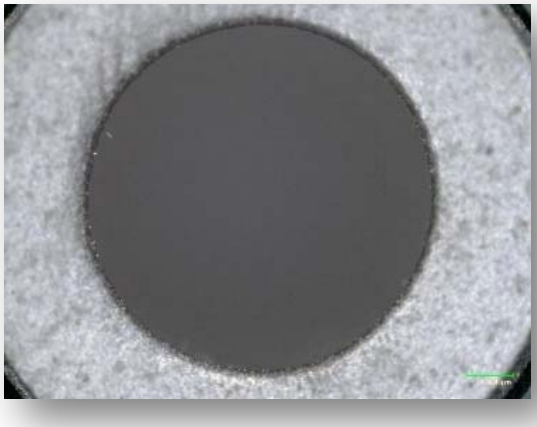
Etching shorts on 01005 chip component pads, the remaining copper has been plated over with nickel and then gold. With finer spacing between small pads this defect can occur but less likely if the boards did go through AOI. Unfortunately, an engineer decided they were only simple test boards for the author so did not check the batch. The same problem has been experienced on smaller chip component footprints like 0402 metric. In addition, when doing etching of both 01005 and 0402 we have also seen loss of pads. We know that copper adhesion to laminate is not as good as it was but losing the pads during etching!!

Poor Wetting on OSP



Incomplete wetting on a surface mount pad is due to contamination on the surface of the pad. In this case the contamination is most likely to be solder mask residues. Although the copper OSP coating process was successful the solderability of the pad has been affected by poor PCB manufacture. Any solderability test or solder float test should show this problem up prior to shipment to the customer. With use of photo definable solder mask this is less of an issue today unless solder mask imaging, development and rinsing is not controlled

Tin Whisker

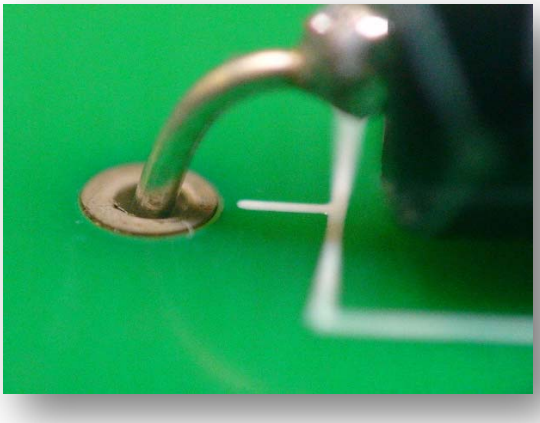


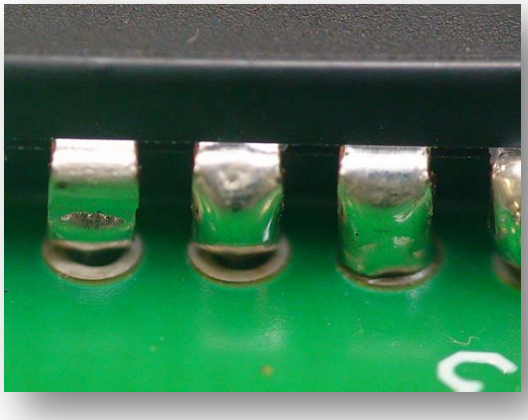
Two examples of tin whisker growth on tin finish boards, you must have good eye sight to spot these. These examples were found on the surface of assembled boards. We have also seen much longer whiskers on boards as supplied by producers. Previous assessment has also shown tin whiskers on the surface of a plated through hole printed circuit board coated with tin. The boards were produced and shipped to a manufacturing site in Europe and, when examined prior to assembly, found to have whisker growth. Tin has become popular on printed boards as one of the alternative coatings; tin has also become the finish of choice in the component manufacturing industry. However, many people have shown concerns over the formation of whiskers, the author on the long term solderability of the finish and its viability for double sided soldering with long hold times between reflow or second stage soldering

There has been a considerable amount of work and technical articles produced on whisker formation and the potential for failure in electronics. There is still a lot of work being undertaken around the world on this subject. The reasons are that we still do not have guaranteed whisker free products or the process where the chemistry is being used is not being maintained correctly. If you follow guidelines on designing a whisker free process and use materials that should not form tin whiskers, somehow, they still appear. This problem is not specifically a lead-free issue as it has been around for years as a possible problem. The increasing use of tin as a component finish and printed board alternative coating has highlighted the potential for failure.

Organisations like NEMI and JEDEC have provided guidelines on what causes whisker formation, ways of accelerating testing for whisker formation and preventative strategies. The team at NPL in Teddington have produced may reports on the tin whisker formation which can be downloaded free at http://defectsdatabase.npl.co.uk

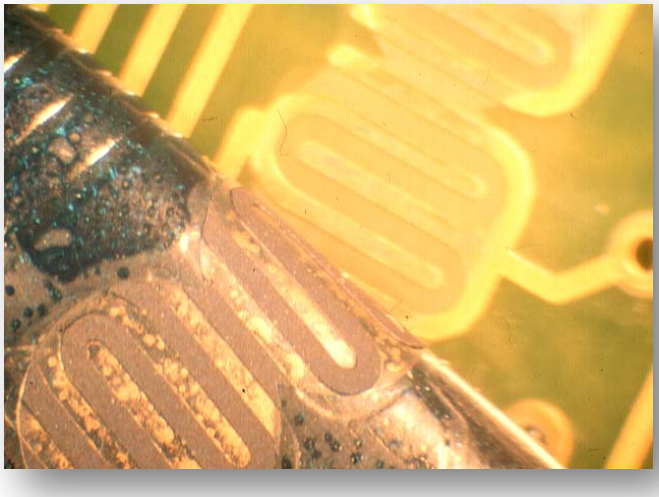
Poor Through Hole Fill





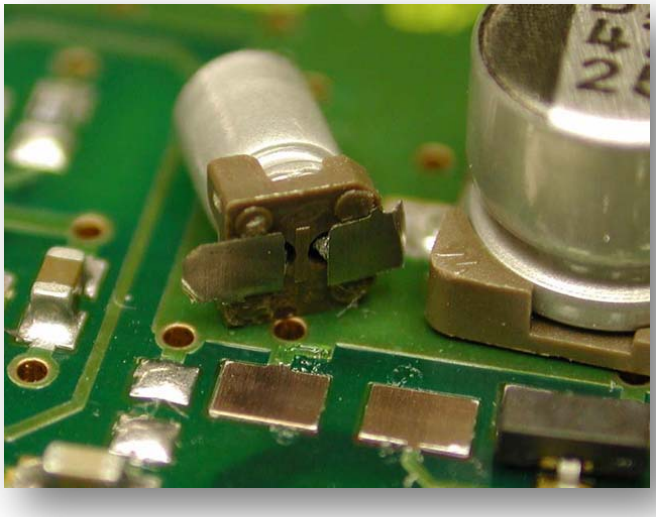
The solderability on this board shows a total lack of through hole solder fill. On the dual in line leads the solderability of the leads was perfect which has allowed the solder to reach the top sided of the board with hand soldering without wetting the barrel of the plated through hole board. This is an example of a tin board which was clearly stored too long before assembly. There are many benefits of different surface finishes in industry but users must understand the options and how to control their supply and storage conditions

Gold Peeling



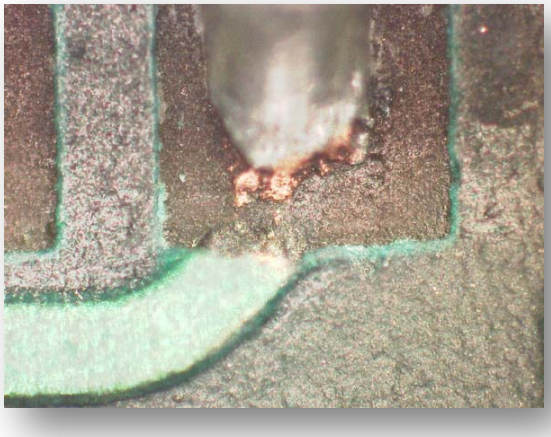
Peelable masking has been used in the past to protect gold key pads during soldering or from solder spitting during reflow which leads to solder wetting spots on some terminals. This in turn may be a cosmetic issue but also may affect the operation of the contacts. In the example the peelable coating has shown up poor adhesion of the gold to the surface of the pads. This problem is related to the preparation of the contact pads prior to gold plating and was not related to the assembly process. Testing for gold adhesion using IPC methods showed a total lack of adhesion

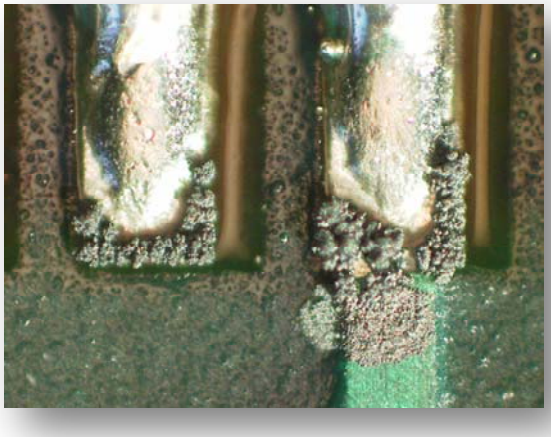
Open Circuit



Solder joint failure has occurred due to the surface finish. The bulk of the solder on the capacitor terminations has just peeled from the pads. During reflow the solder paste has spread and wet the surface of the pad coating and the terminations. The solder has wet and dissolved the gold but then failed to wet the underlying nickel. The failure would be related to the original surface coating or the pad preparation on the PCB and is not an assembly and soldering failure. In this case it was poor control of the nickel plating process, the gold was porous and the nickel penetrated to the surface of the gold

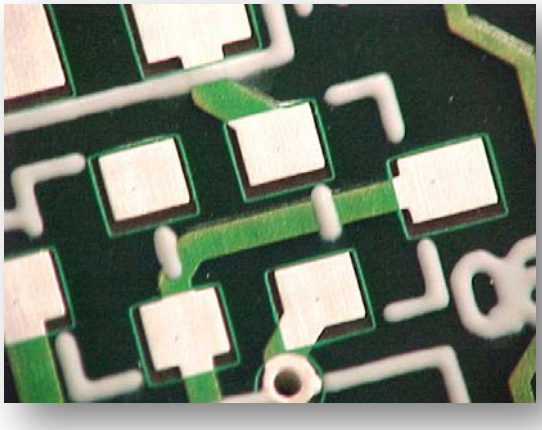
Open Circuit





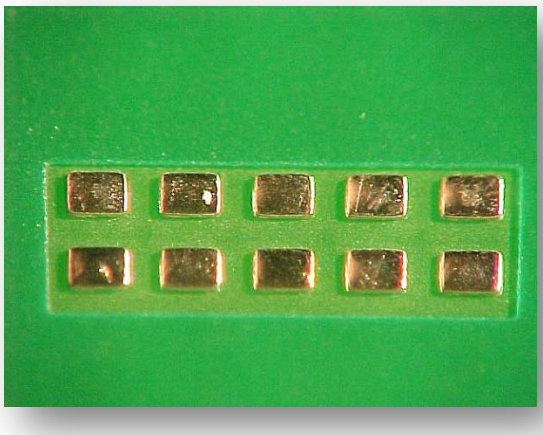
The tracks leading to the surface mount terminations are missing, during operation of the equipment the copper has been eroded. In this case the board was exposed to high levels of sulphur and the combination of copper and silver at the pad interface has resulted in significant sulphur corrosion leading to open circuits. There have been many examples of this type of failure during the introduction of lead-free without lead-free solder being specifically the cause of the problem. Suppliers of silver chemistry have been able to improve the processes used and help producers to minimise this particular problem. However, many silver users that did experience problems did relook at the coatings for this type of demanding environment and switched to solder level or gold over nickel

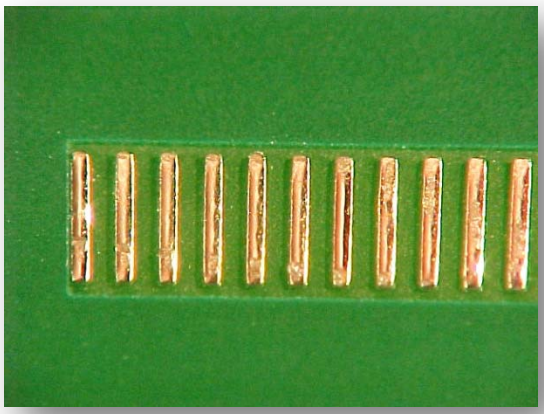
Satisfactory Coating



PCB is visually satisfactory after being cleaned after unsatisfactory solder paste printing step. However, the solderability of the finish may be affected. It is important to evaluate the impact of your cleaning process on any surface finish you may be considering, to avoid process problems in the future. Marking the boards to show they have been cleaned is good practice for future tractability, its normal to just mark the edge with a felt tip pen to be easily seen during inspection and to avoid time consuming investigation. When setting up a printer and printing the first board can be very easily done without putting paste on a board. Simply use low tack clear film is used on a set up board held for the purpose. Perfect print and alignment can be confirmed with SPI measurements made on film

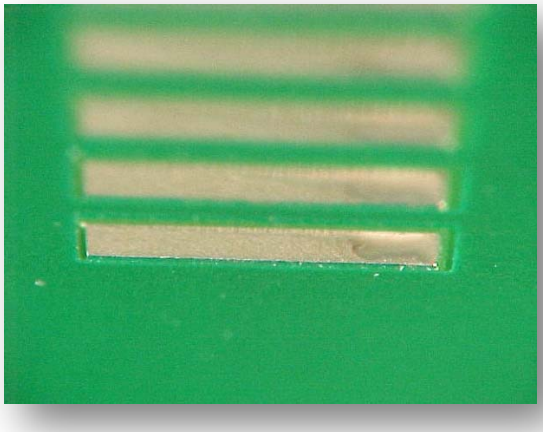
Solder Levelled Surface

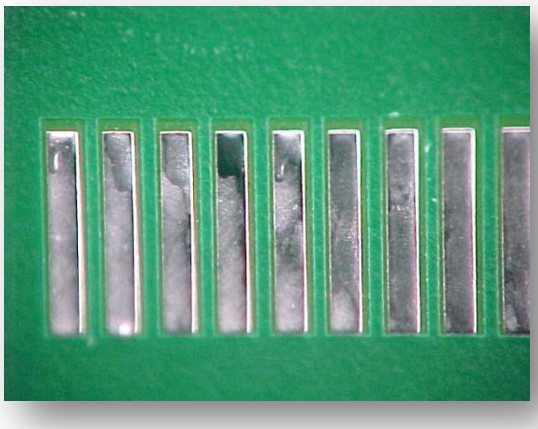




Solder levelling has been a common process for tin/lead and also lead-free and depending on the supplier. The coating can work well for fine and standard pitch products with careful set up of the process. Solder levelling has had a bad name in some cases due to the limited amount of process engineering. Selecting the right combination of solder, flux and some experimenting the variation in solder coating thickness can be decreased. If the coating thickness variation can be reduced there will be less impact on printing, placement and potential yield. The two example groups of pads on the author's test boards are typical from a good supplier. In this case tin/copper/nickel alloy was used during levelling

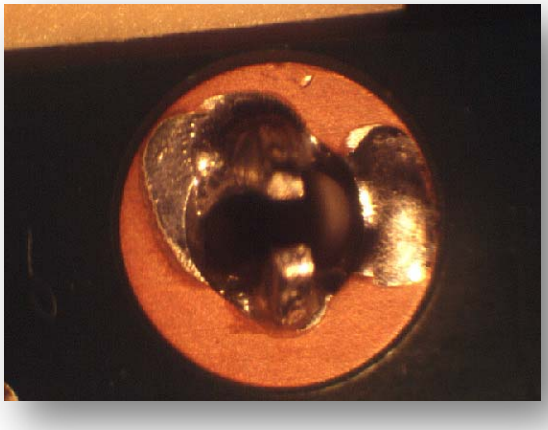
Solder Levelled Surface

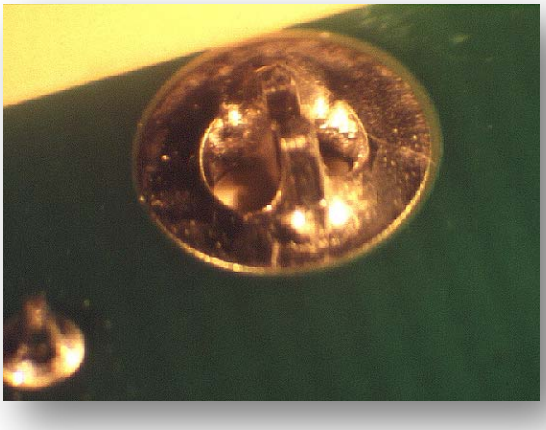




The examples on 0.020" pitch pads show the droplet formation on the surface of solder levelled boards due to air knife pressure used to remove excess solder from the pads. This variation is considered minor and the board would remain solderable for six months in normal storage. With correct solder paste printer set up this would not impact the printing or place of parts on the board. If you are going to specify a solder levelled coating confirm the alloy and thickness variations. Don't just specify lead-free solder levelling as many users do

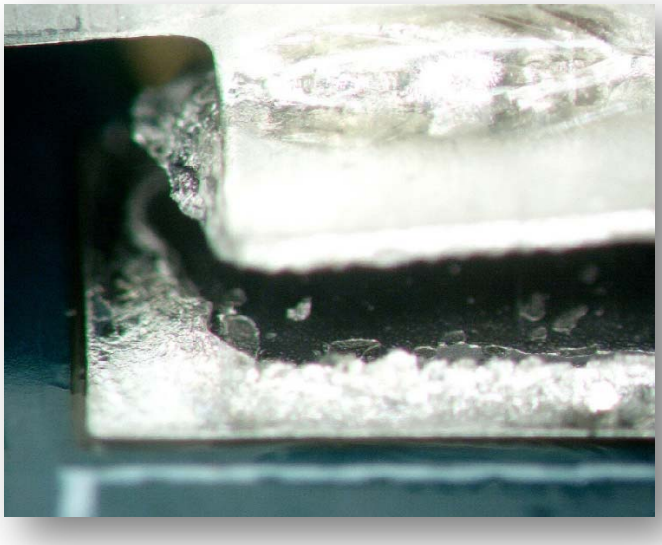
Incomplete Through Hole Fill





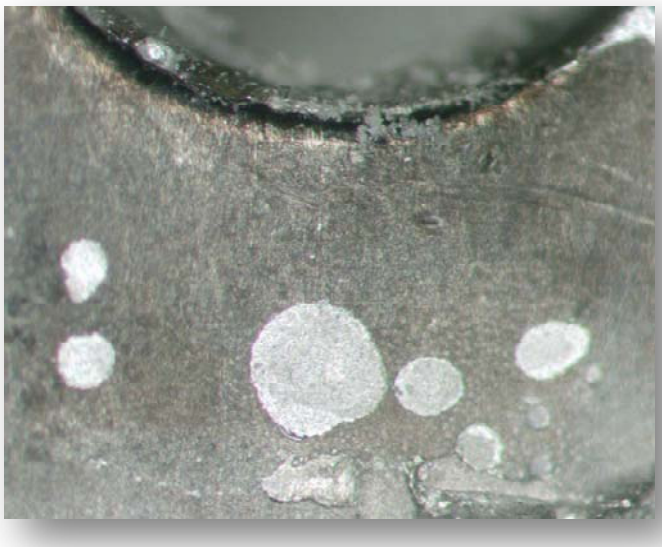
Here are two through hole connection/hold down pins on a connector. The first example on the left is copper OSP and the example on the right is a solder levelled finish. Both pins and holes have not been completely filled with solder in an intrusive reflow process where paste is used to fill the hole during reflow. In both cases there was not the volume of solder paste to be able to fill the hole and reflow out to wet the complete pad surface. In both cases the strength of the joint was more than the retention force of the pin in the connector body, the pins failed not the joint. With intrusive reflow with a hole of this size its not possible to fill the hole but good reliable joint can be produced. Further reference on pin in hole reflow can be obtained from the author's free E-book http://www.pihrtechnology.com/pdf/PIHR-Book.pdf

Solder Joint Failure



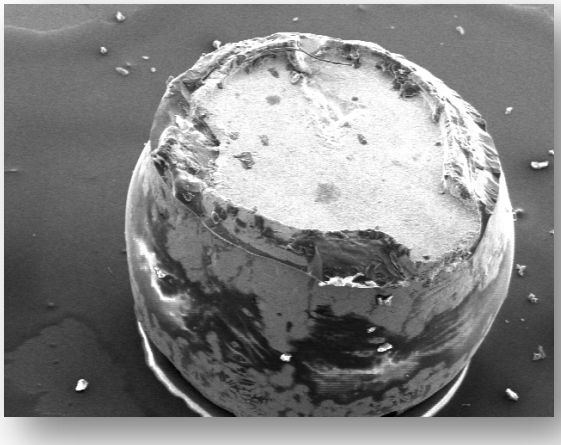
Solder joint failure due to the surface finish, the bulk of the solder on the component termination has separated from the pad after assembly. As the image shows, during reflow the solder paste has reflowed fully across the surface of the pads forming what visually would be a perfect joint. However the solder has failed to make a reliable connection. Investigation showed wetting to selected areas of the pads without fully wetting and forming an intermetallic layer across the joint

Solder Joint Failure



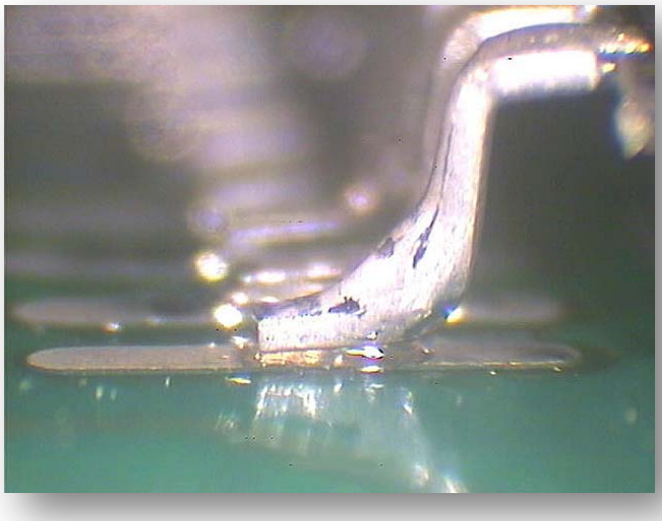
Surface of the pad on the joint failure above showing virtually no wetting or intermetallic bond. The solder around a plated through hole also shows evidence of separation from the base copper and is related to the PCB manufacturing process rather than any soldering operation

BGA Solder Joint Failure



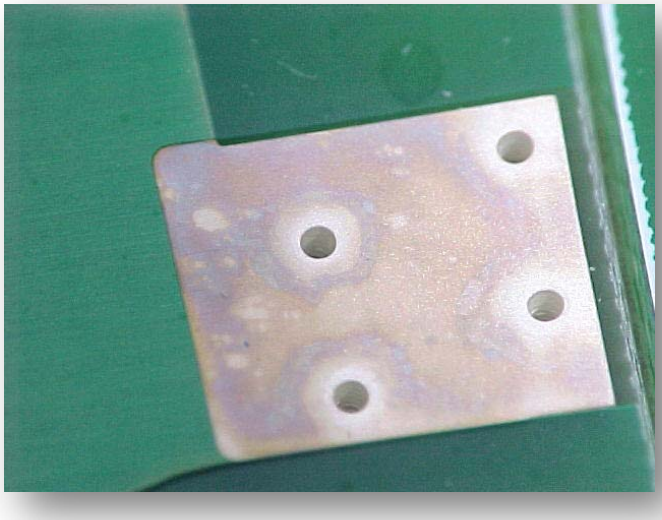
Dye and pry testing on area array components is a common process to show cracking in joints or complete open joints at the PCB or component interface. The example shows 100% dye penetration and failure of the ball termination. Solder has reflowed and dissolved the gold but has not wet the nickel surface under the gold allowing the dye to penetrate. The SEM image shows a close up of a BGA joint, cleanly separated from the pad on the PCB surface as the outline of the pad and the track leading to the pad is visible

Solder Wicking



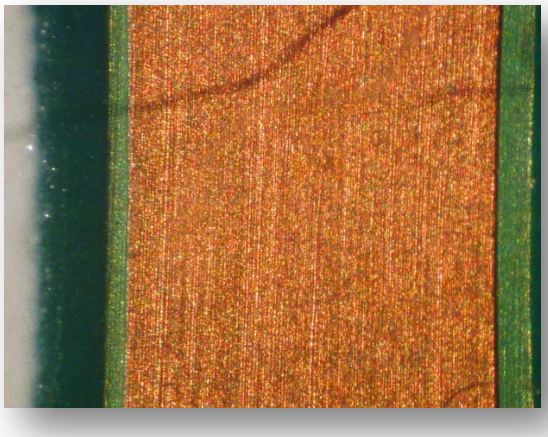
Solder wicking is visible on this gull wing termination. All the solder paste has reflowed successfully on the pad surface but failed to wet the pad. The pin was highly solderable, all the solder volume has wicked up the pin. Sometimes this is surface coating related, contamination from the PCB supplier or assembly related. This type of defect can be seen on most surface finishes and can relate simply to a difference in wetting times between the two surfaces to be joined and is sometimes exaggerated using nitrogen reflow or vapour phase

Coating Discoloration



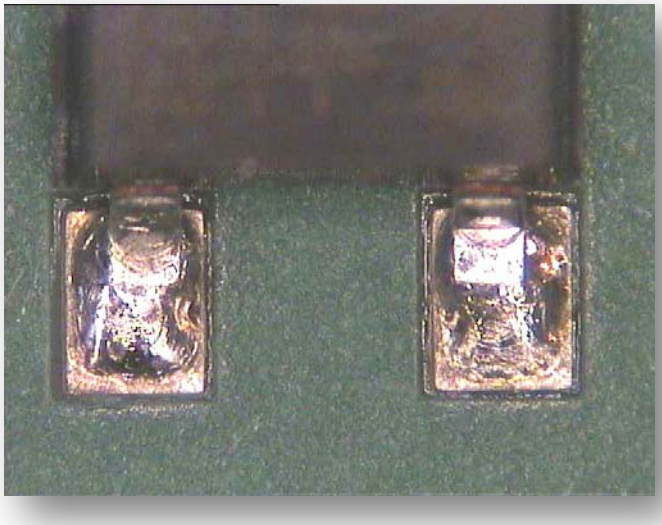
Tin and silver coatings can often have drying/oxide marks like the colours of the rainbow. This can be all over the board, only on the top and bottom of a stack of recently opened boards or on selected groups of pads depending on the cause. Often the solderability is not affected but this still is a cause for concern. Wetting indicator pads, if available, are a simple way of testing a sample board from the batch to gain acceptance. A shop floor solder paste reflow test is an ideal way of testing and giving confidence in the batch of boards to be assembled. The author has used a simple dot test pattern for many years and the design, and procedures for use are available on request from technical@smartgroup.org

Poor Surface Preparation



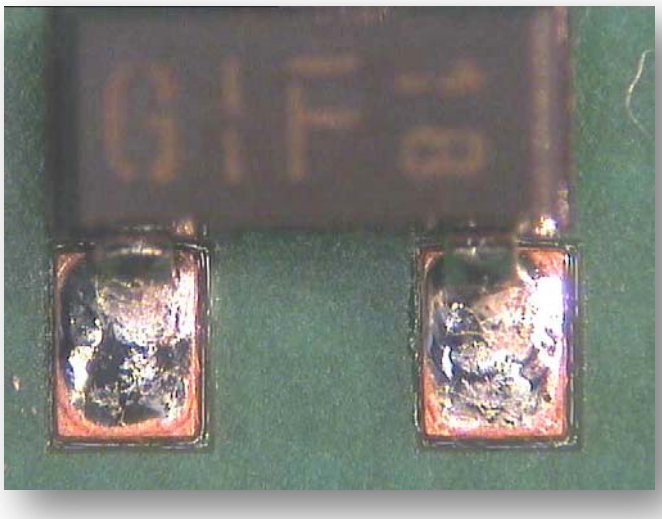
Any surface coating does not perform as well if the copper surface below is subjected to a mechanical cleaning operation. The score marks on the surface of the pad are plainly visible on this copper OSP board. The poor surface treatment of the copper surface has been shown to impact the storage life of organic coatings as well as tin and silver and should be investigated. The mechanical cleaning marks are less obvious on the pad of the silver finish sample shown on the right

Reduced Solder Wetting



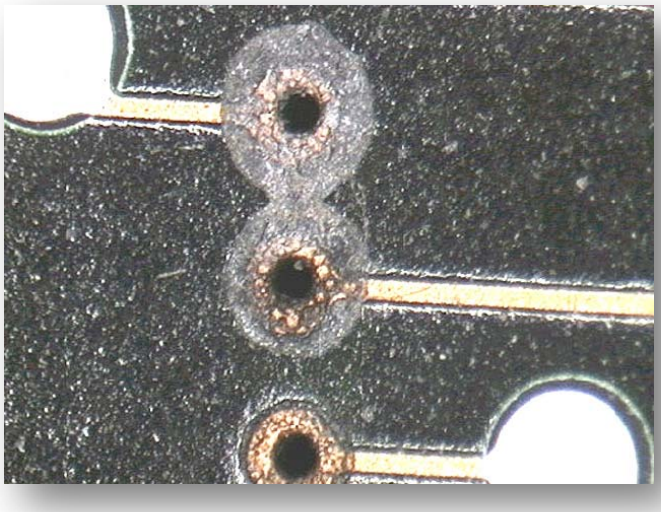
In a lead-free soldering process the degree of solder coverage may be reduced based on the solder finish, size of paste aperture printed, activity of the flux and the profile. In this case the solder has not wetted to the edge of the pad surface. However, a perfectly sound solder joint has been produced. When moving to alternative surface finishes the change in joint appearance must be understood by all departments to avoid unnecessary rework or rejection. It should also be understood by customers who are subcontracting products, exposed base material is not always an issue and is covered in IPC 610 Acceptability of Electronic Assemblies and IPC 600 Acceptability of Printed Circuit Boards

Reduced Solder Wetting



The choice of surface finish on a printed board will have an impact on degree of solder spread in tin/lead and lead-free assembly. The solder in the example has not wet over the full surface of the copper OSP pad but has formed a satisfactory joint. Exposed copper in many applications will not impact reliability; however, the difference in appearance, if not expected, can be an emotive subject with some customers

Surface Corrosion

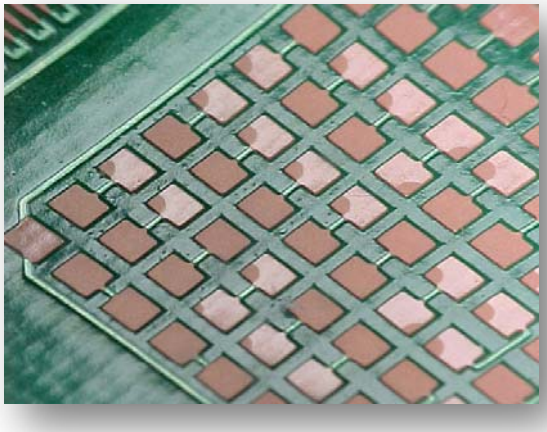


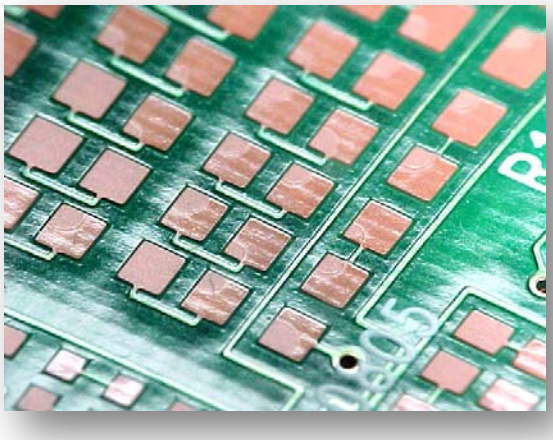
Corrosion deposits are visible around via holes on a product returned from the field. This could be related to creep corrosion due to the impact of sulphur and the product's working environment or trapped chemicals in the via holes not removed during manufacture. Surface analysis should be able to determine the failure type and is quite a common problem seen in industry, even if it does not cause immediate failure of a product

Copper Dissolution

The solder pad is missing from the through hole joints, a typical assumption would be poor rework. However, the pad has been dissolved during lead-free soldering. This can be due to a combination of the solder alloy, temperature, soldering time and solder flow rate. All surface finishes except for nickel/gold are susceptible to copper erosion. Solder levelling with some lead-free alloys can also reduce the copper thickness significantly even before the assembly operation and needs to be monitored. This problem was first seen on lead free rework using solder fountains then experience with selective soldering before the problem was full examined. NPL has two documents specifically looking at copper dissolution during soldering with different lead-free alloys and can be downloaded Free http://defectsdatabase.npl.co.uk

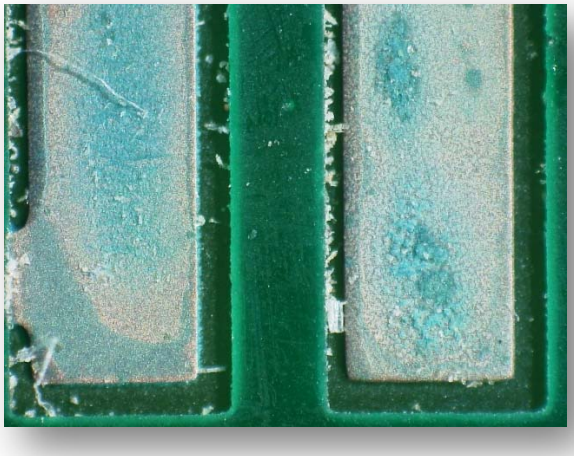
Inconsistent Copper Coating





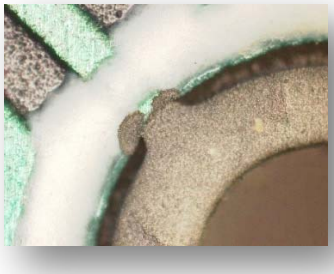
The copper OSP coating process has failed to provide a consistent coverage on the board on the left which will lead to soldering problems. A reference to a typical coated surface is provided at the front of this guide and can be used as a reference for inspection. Alternatively, a company should hold their own reference boards or images for goods in inspection. Boards found like this at goods in inspection should be rejected. The example on the right is a lacquer coating, poorly coated but not often used today in PCB manufacture unless on single sided through hole boards. the lacquer coating is not a good option for surface mount boards that are wave soldered due to solder joint skipping

Uneven Print Surface



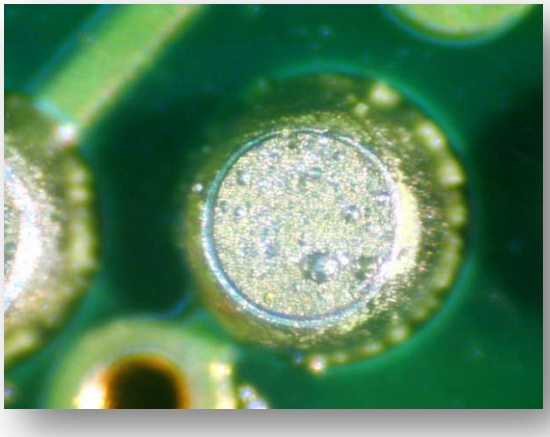
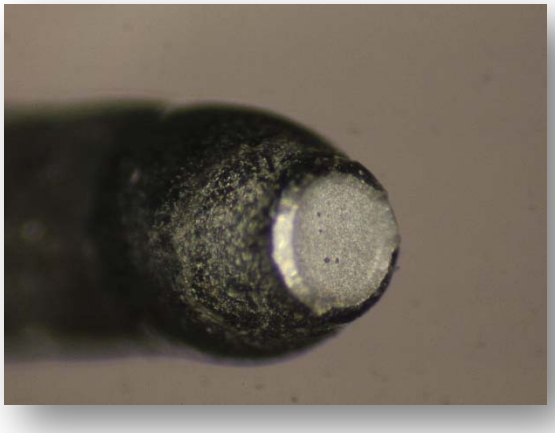
Solder mask residues are visible on the surface of the pads and may have been the result of a poorly controlled development and rinsing process, the imaging of the solder mask is well defined but with some undercutting of the solder mask. Ideally you will always have vertical side walls to avoid contamination and solder residues. Removing the residue showed the base pad surface

Surface Corrosion



Tracks leading to the surface mount terminations are reduced, during operation of the equipment the copper has been eroded. In this case the board was exposed to high levels of sulphur and the combination of copper and silver at the pad interface has resulted in significant sulphur corrosion leading to open circuits. There have been many examples of this type of failure during the introduction of lead-free without lead-free solder being specifically the cause of the problem. Suppliers of silver chemistry have been able to improve the processes used and help producers to minimise this particular problem. However, many silver users that did experience problems did relook at the coatings for this type of demanding environment and switched to solder level or gold over nickel

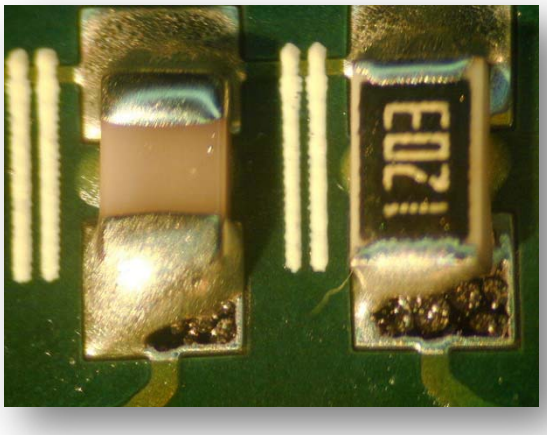
Champagne Voiding

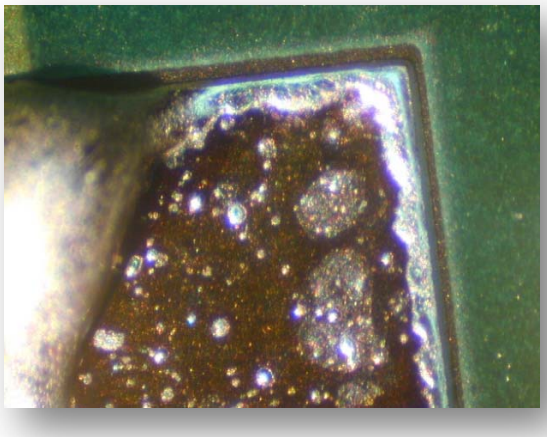



Voids in the solder joints are not uncommon after reflow soldering and can be easily detected using x-ray. Champagne voiding is related to hundreds of very small voids seen at the solder joint to surface pad interface. Normally in reflow voiding may be related to the paste and profile. The voids will be seen in the bulk of the solder joint or near the top of the joint at the component pad interface. Champagne voiding was originally seen on silver coated boards and related to the organics gassing during reflow soldering. This problem was overcome by both chemistry suppliers to the industry. However, the author has seen a few recent cases in one automotive supplier

The second image on the right shows a ball pull test conducted on a DAGE heated stage to examine pad cratering between PCB pads and laminate but has also be used by the author to examine voiding on joint interfaces. It may be possible to compare the degree of voiding at the interface with joint strength. The ball pull test can be very valuable to assess the impact on joints

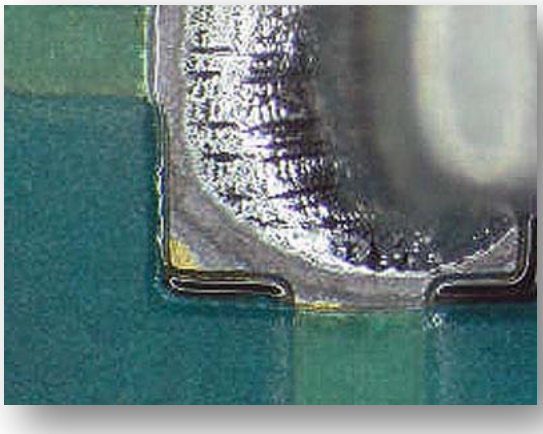
Black Tarr





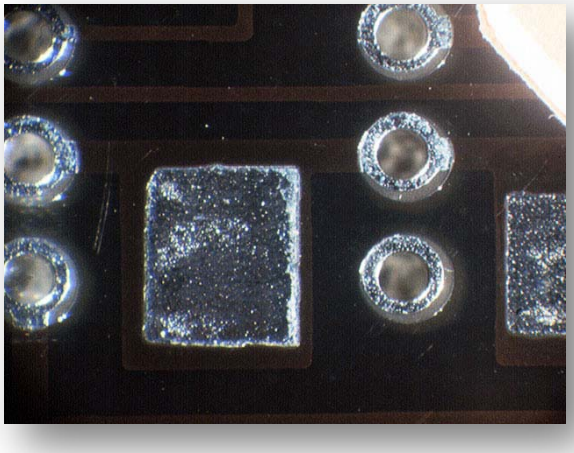
Black Tarr was a term coined by two UK Engineers in our industry to try and describe a defect to avoid the confusion with Black Pad related to gold over nickel boards. Black Tarr is still seen on gold over nickel surface finish boards but its not related to the surface attack of the nickel at the grain boundary. Black Pad tends to reduce the areas of satisfactory contact at the junction of the nickel grain boundary. Black Tarr is always seen as a coating like deposit on the surface of the nickel after soldering when the gold has been dissolved into the bulk of the joint

Incomplete Wetting



Solder paste has reflowed on the surface of the pad, consuming the gold and wetting to the nickel surface. The reduced wetting and coverage of the pad is related to the limited volume of the solder paste on the pad

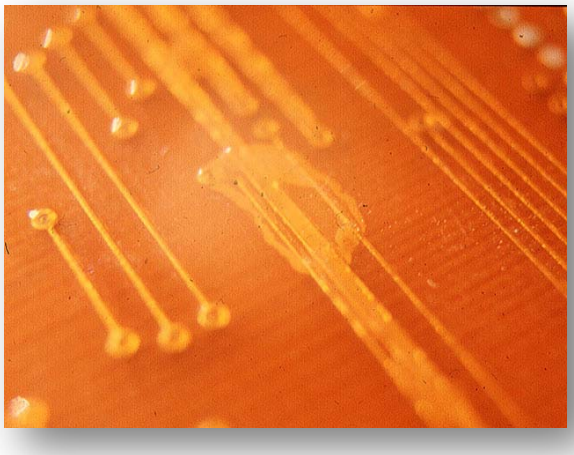
Surface Texture of Levelled Pads



The board has been through a solder levelling process where the solder bath was contaminated with a high level of copper. Copper is the element most commonly seen to contaminate a solder bath in PCB manufacture. During the levelling process the tin in the tin/lead solder dissolves the copper surface which is quite normal as this is how a solder joint is formed. The dissolution of copper is exaggerated with the use of different lead-free solder alloys. This in turn is increased due to the temperature, immersion time and solder flow rate over the copper surface

When a solder levelling system is being used continuously the copper content in the bath will slowly build up. As bare copper is going into a levelling system the build-up will appear faster than on a traditional wave soldering process. When the solder bath has a copper concentration of over 0.2% for tin/lead solders it starts to influence the drainage of the solder from the board and over 0.25% it starts to show up as a granular appearance. Normally suppliers will change or dilute their bath or remove the copper before this can occur. Suppliers will have developed their own standards for different lead-free alloys and will also look at ways of dredging the bath to remove the copper/tin needles

Flexible Coverlay Lifting

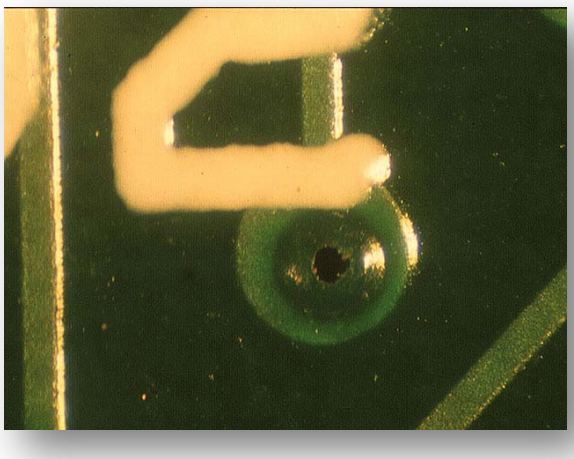


Solder levelling of flexible circuits normally requires a prebake of the circuit. Flexible circuits are made of polyimide and are far more prone to water absorption than normal epoxy/fibreglass substrates. Experience shows that baking can be avoided on single and double sided polyimide flexibles when a liquid solder mask is used as an alternative to a polyimide coverlayer

A bake cycle of 1 hour at 110-120^{o}C is normally required to eliminate this problem occurring. All the circuits must see the correct time and temperature hence the oven must be checked for good temperature stability, the correct loading and proper extraction. It should not be used for other applications like resist and legend curing or other curing operations.

To confirm that the bake cycle is correct for any circuit board it is possible to establish the correct temperature time bake cycle. This is achieved by a weight gain weight loss test, it is difficult and time consuming to do and you need a special environment and accurate scales. IPC have a specification on PCB storage and provides basic information on baking circuit boards

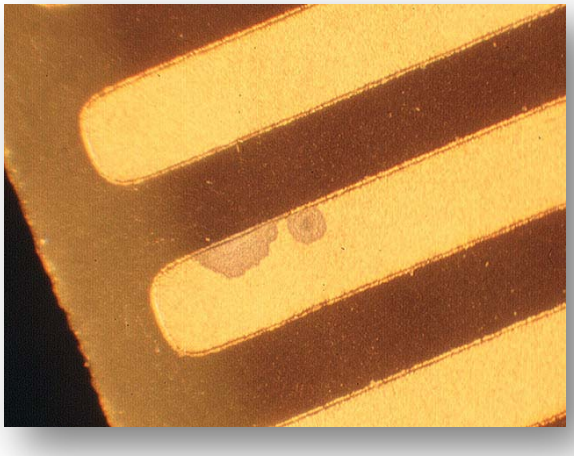
Via Holes Popping



When solder mask is applied over a via hole sealing the barrel outgassing can cause the resist to pop during solder levelling. The resist blister may seem just a cosmetic problem but it can affect solder paste printing on fine pitch boards. The resist locally lifts the stencil from the surface of the board. The appearance of lifting or cracking of the solder mask may be affected by the type of mask, one that is either brittle or flexible

Gassing may occur during solder levelling, reflow soldering and wave soldering. Wave soldering should be less of a problem but second side reflow would be an issue for the process engineer. Either the air trapped in the barrel of the hole or outgassing from the hole wall will cause this problem and it can also cause solder balls on the top of vias if the levelling process is attempting to fill the vias. In high reliability applications and thickness multilayer boards vias are sometimes filled with epoxy then capped with solder mask. However, experience shows that vias can still outgas during reflow

Solder on Gold Pads



There are occasions when boards which feature gold pads need to be solder levelled. This has of course changed over the last few years as design engineers requiring gold contacts have tended to move to nickel/gold coated boards. This will depend on the specification for the gold contacts as standard nickel/gold used for soldering will allow limited connector mating without thick plated gold

When a company prefers tin/lead as a solderable surface but needs gold contacts for other forms of interconnection levelling can be used. Care needs to be taken on the protective coating applied to the board to stop solder spotting.

Spotting occurs when small balls of solder are present on the surface of the gold pads. In a liquid state, they wet the surface and spread significantly. The masking process and the thickness of the masking needs to be reviewed carefully. It is more common to see solder spotting on nickel/gold boards in assembly where solder paste particles have contaminated gold pads

PCB Surface Finishes & Solderability Standards & Text Books

IPC-4552 Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards
IPC-4553 Specification for Immersion Silver Plating for Printed Boards
IPC-4554 Specification for Immersion Tin Plating for Printed Circuit Boards
IPC-4555 Specification for Organic Solderability Preservative (OSP) for Printed Circuit Boards (Committee Draft)
IPC-4556 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) Plating for Printed Circuit Boards

IPC J-STD 003 Solderability Tests for Printed Boards
IPC 600 Acceptability of Printed Circuit Boards
IPC 610 Acceptability of Electronic Assemblies

In addition, a specification for solder levelled boards is required as well as other new finishes

The following are text books on printed board manufacture which include details on surface finish

Printed Circuit Handbook (7th Edition and the PCB Manufacturing Bible)
Clyde Coombs, Jr. - McGraw Hill

Flexible Circuit Technology 4th Edition
Joe Fjelstad – BRP (Free Download)

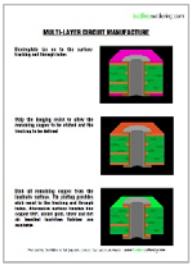
Comprehensive Guide to Design, Manufacture of Printed Board Assemblies
Bill MacLeod Ross - Electrochemical Publications (Finishing Publications Limited)

Quality Assessment of Printed Circuit Boards (Out of Print search on-line its worth it)
Preben Lund - Bishop Graphics Inc.

SMT for PC Board Design (2nd - 3rd Edition)
James Hollomon - Prompt Publications

PCB Training Material & Services

Over the last few years we have created several products and services for PCB manufacture and solder finish education which are commercially available worldwide. These products and services are based on practical experience and evaluation projects conducted by the author. Any of these products or services can be obtained by contacting info@smartgroup.org or in the case of CD-ROM and poster sets they can be obtained from other industry groups. SMART provides onsite training and online webinars on coating and defect prevention



PCB CD training products, photo CD and sets of inspection charts shown above can be obtained from the following organisations or websites. SMART Group can also run theory and hands on workshops or online webinars for your company:

SMART Surface Mount & Related Technologies Association
www.smartgroup.org

SMTA Surface Mount Technology Association
www.smta.org

IPC
www.ipc.org

For further information on products or to book a workshop or webinar contact info@smartgroup.org

Workshops/Webinars on PCB Manufacture & Surface Finishes

SMART Group offer onsite training courses or online webinars for member companies. The length or the delivery method of training can be adapted to suit your team and location. For further information contact SMART Group office info@smartgroup.org

Printed Circuit Board Solderable Finishes for Fine Pitch & Lead-Free Assembly

Practical Solderability Testing for PCBs & Components

PCB Inspection & Quality Assessment – Practical Solutions

Printed Circuit Board Failures – Causes and Cures

PCB Microsectioning & Analysis of Failure Quality Standards

Guide to Basic Printed Board Manufacture for Purchasing Engineers

Author's Profile

Bob Willis currently operates a training and consultancy business based in UK and has created one of the largest collections of training material in the industry. He is a member of the SMART Group Technical Committee. Over the years Bob has been Chairman and Technical Director of the SMART Group and holds the title of Honorary Life Vice President for his contributions to the Group since its inception. With his online training webinars Bob Willis provides a cost effective solution to training worldwide and regularly runs training for SMTA, SMART, IPC and recently EIPC. Although a specialist for companies implementing lead-free manufacture Bob has provided worldwide consultancy in most areas of electronic manufacture over the last 30 years. Bob has travelled in the United States, Japan, China, New Zealand, Australia, South Africa and the Far East consulting and lecturing on electronic assembly

Bob was presented with the *"Paul Eisler award by the IMF (Institute of Metal Finishing)"* for the best technical paper during their technical programmes. He has conducted SMT Training programs for Texas Instruments and ran Reflow and Wave Soldering Workshops in Europe for one of the largest suppliers of capital equipment. This is based on many years of practical experience working in telecommunications, military OEM, contract assembly, printed board manufacture, environmental test and quality control laboratories. This has earned him the *SOLDERTEC/Tin Technology Global Lead-Free Award* for his contribution to the industry. He has also been presented with the *SMTA International Leadership Award* and *IPC Committee Award* for contribution to their standards activity

He has also run training workshops with research groups like *ITTF, SINTEF, NPL & IVF* in Europe. Bob has organised and run lead-free production lines at international exhibitions *Productronica*, *Hanover Fair*. *Nepcon Electronics* in Germany and England plus IPC APEX and SMTA International in USA providing an insight to the practical use of lead-free soldering, high temperature electronics, cleaning, conformal coating on Ball Grid Array (BGA), Chip Scale Package (CSP), 0210 chip and through hole intrusive reflow connectors. In September 2016 Bob was presented with *Best Speaker at SMTA International Conference* 2016 in Chicago

He has worked with the GEC Technical Directorate as Surface Mount Co-Ordinator for both the Marconi and GEC group of companies and prior to that he was Senior Process Control Engineer with Marconi Communication Systems. Following his time with GEC he became Technical Director of an electronics contract manufacturing company where he formed a successful training and consultancy division